

### FEATURES

- Worldwide NTSC/PAL/SECAM color demodulation support
- One 10-bit analog-to-digital converter (ADC), 4× oversampling for CVBS, 2× oversampling for Y/C mode, and 2× oversampling for YPrPb (per channel)
- Four analog video input channels with on-chip antialiasing filter CVBS (composite), Y/C (S-Video), and YPrPb (component) video input support
- Fully differential, pseudo differential, and single-ended CVBS video input support
- Up to 4 V common-mode input range solution
- Excellent common-mode rejection capabilities
- Five-line adaptive comb filters and CTI/DNR video enhancement
- TBC functionality provided by adaptive digital line length tracking (ADLLT), signal processing, and enhanced first in, first out (FIFO) management
- Integrated automatic gain control (AGC) with adaptive peak white mode
- Video fast switch capability
- Adaptive contrast enhancement (ACE)

- Down dither (8 bits to 6 bits)
- Rovi™ (Macrovision) copy protection detection
- NTSC/PAL/SECAM autodetection
- 8-bit ITU-R BT.656 YCrCb 4:2:2 output and HS, VS, or FIELD
- Full-featured VBI data slicer with teletext support (WST)
- Power-down mode and ultralow sleep mode current
- Two-wire serial MPU interface (I<sup>2</sup>C compatible)
- Single 1.8 V supply possible
- Qualified for automotive applications
- −40°C to +105°C temperature grade
- 32-lead, 5 mm × 5 mm, RoHS-compliant LFCSP

### APPLICATIONS

- Automotive infotainment
- DVRs for video security
- Media players

### FUNCTIONAL BLOCK DIAGRAM

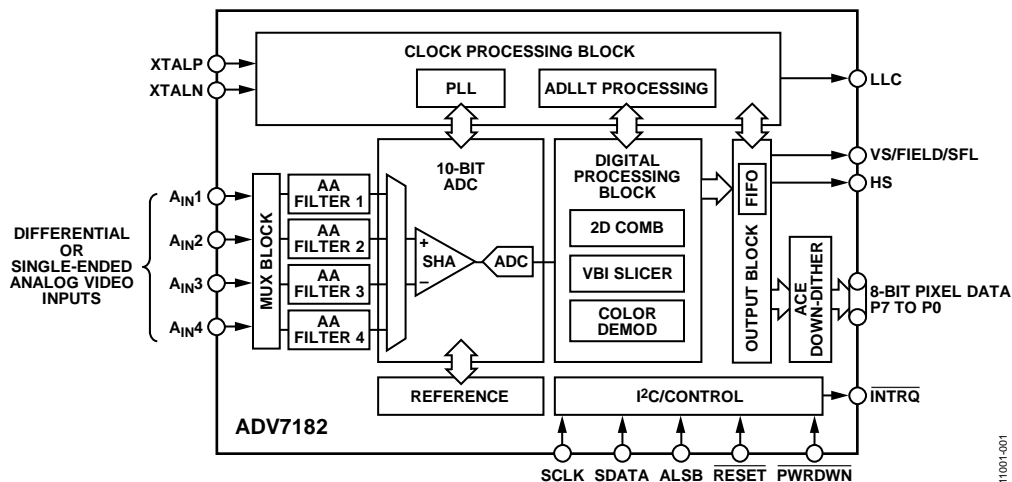


Figure 1.

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## REVISION HISTORY

1/13—Revision 0: Initial Version

## GENERAL DESCRIPTION

The [ADV7182](#) automatically detects and converts standard analog baseband video signals compatible with worldwide NTSC, PAL, and SECAM standards into a 4:2:2 component video data stream. This video data stream is compatible with the 8-bit ITU-R BT.656 interface standard.

External HS, VS, and FIELD signals can provide timing references for LCD controllers and other video ASICs. The accurate 10-bit analog-to-digital conversion provides professional quality video performance for consumer applications with true 8-bit data resolution. The analog video inputs accept both single-ended, pseudo-differential, and fully differential composite video signals as well as S-Video and YPbPr video signals, supporting a wide range of consumer and automotive video sources.

The [ADV7182](#) along with an external resistor divider provide a common-mode input range of 4 V, enabling the removal of large signal, common-mode transients present on the video lines. Common-mode rejection (CMR) values of up to 80 dB can be achieved without the need for external amplifier circuitry.

The AGC and clamp restore circuitry allow an input video signal peak-to-peak range to 1.0 V at the analog video input pin of the [ADV7182](#). Alternatively, these can be bypassed for manual settings.

The [ADV7182](#) can be protected from short-to-battery (STB) events with standard ac coupling capacitors.

The line-locked clock output allows the output data rate, timing signals, and output clock signals to be synchronous, asynchronous, or line locked even with  $\pm 5\%$  line length variation.

The [ADV7182](#) is programmed via a two-wire, serial bidirectional port (I<sup>2</sup>C<sup>®</sup> compatible) and is fabricated in a 1.8 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The LFCSP package options make the decoder ideal for space-constrained portable applications.

The [ADV7182](#) is a versatile one-chip multiformat video decoder that automatically detects PAL, NTSC, and SECAM standards in the form of composite, S-Video, and component video. The [ADV7182](#) can receive composite signals in either single-ended or differential modes. This makes the [ADV7182](#) ideal for automotive applications.

The [ADV7182](#) converts these analog video formats into a digital 8-bit ITU-R BT.656 video stream.

The digital video output stream of the [ADV7182](#) interfaces easily to a wide range of MPEG encoders, codecs, mobile video processors, and Analog Devices, Inc., digital video encoders, such as the [ADV7391](#). External HS, VS, and FIELD signals provide timing references for LCD controllers and other video ASICs.

## OVERVIEW OF THE ANALOG FRONT END

The [ADV7182](#) analog front end (AFE) comprises a single high speed, 10-bit ADC that digitizes the analog video signal before applying it to the standard definition processor. The AFE employs differential channels to the ADC to ensure high performance in mixed-signal applications and to enable differential CVBS to be connected directly to the [ADV7182](#).

The front end also includes a 3-channel input mux that enables multiple composite video signals to be applied to the [ADV7182](#). Current clamps are positioned in front of the ADC to ensure that the video signal remains within the range of the converter. A resistor divider network is required before each analog input channel to ensure that the input signal is kept within the range of the ADC (see Figure 23). The choice of this resistor divider ratio provides a common-mode range of up to 4 V. Fine clamping of the video signal is performed downstream by digital fine clamping within the [ADV7182](#).

Table 1 shows the three ADC clocking rates that are determined by the video input format to be processed. These clock rates ensure 4× oversampling per channel for CVBS, Y/C, and YPrPb modes.

The [ADV7182](#) has a fully differential AFE. This allows for inherent small and large signal noise rejection, improved electromagnetic interference (EMI), and the ability to absorb ground bounce. Support is offered for both true differential and pseudo-differential signals.

**Table 1. ADC Clock Rates**

Input Format	ADC Clock Rate (MHz) <sup>1</sup>	Oversampling Rate per Channel
CVBS	57.27	4×
Y/C (S-Video) <sup>2</sup>	114	4×
YPrPb <sup>2</sup>	172	4×

<sup>1</sup> Based on a 28.63636 MHz clock input to the [ADV7182](#).

<sup>2</sup> See INSEL[4:0] in Table 94 for writes needed to set Y/C (S-Video) and YPrPb modes.

## OVERVIEW OF THE STANDARD DEFINITION PROCESSOR

The [ADV7182](#) is capable of decoding a large selection of baseband video signals in composite (both single-ended and differential), S-Video, and component formats. The video standards supported by the video processor include PAL B/PAL D/PAL I/PAL G/PAL H, PAL 60, PAL M, PAL N, PAL Nc, NTSC M/NTSC J, NTSC 4.43, and SECAM B/SECAM D/SECAM G/SECAM K/SECAM L. The [ADV7182](#) can automatically detect the video standard and process it accordingly.

The [ADV7182](#) has a five-line, superadaptive, 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to the video standard and signal quality without requiring user intervention. Video user controls such as brightness, contrast, saturation, and hue are also available with the [ADV7182](#).

The [ADV7182](#) implements a patented ADLLT™ algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the [ADV7182](#) to track and decode poor quality video sources such as VCRs and noisy sources from tuner outputs,

VCD players, and camcorders. The [ADV7182](#) contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The ACE offers improved visual detail using an algorithm that automatically varies contrast levels to enhance picture detail. This enables the contrast in dark areas of an image to be increased without saturating the bright areas of an image. This is particularly useful in automotive applications, where it can be important to be able to discern objects in shaded areas.

Down dithering from eight bits to six bits enables ease of design for standard LCD panels.

The video processor can process a variety of VBI data services, such as closed captioning (CCAP), wide screen signaling (WSS), copy generation management system (CGMS), and teletext data slicing for world standard teletext (WST). Data is transmitted via the 8-bit video output port as ancillary data packets (ANC). The [ADV7182](#) is fully Macrovision® certified; detection circuitry enables Type I, Type II, and Type III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

$A_{VDD}$ ,  $D_{VDD}$ , and  $P_{VDD} = 1.71\text{ V to }1.89\text{ V}$ ;  $D_{VDDIO} = 1.71\text{ V to }3.46\text{ V}$ , specified at operating temperature range, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	CVBS mode		2		LSB
Differential Nonlinearity	DNL	CVBS mode		-0.6/+0.6		LSB
DIGITAL INPUTS						
Input High Voltage (DVDDIO = 3.3 V)	$V_{IH}$		2			V
Input High Voltage (DVDDIO = 1.8 V)	$V_{IH}$		1.2			V
Input Low Voltage (DVDDIO = 3.3 V)	$V_{IL}$				0.8	V
Input Low Voltage (DVDDIO = 1.8 V)	$V_{IL}$				0.4	V
Crystal Inputs	$V_{IH}$ $V_{IL}$		1.2			V V
Input Leakage Current	$I_{IN}$		-10		+10	$\mu\text{A}$
Input Leakage Current (SDATA, SCLK)	$I_{IN}$		-10		+15	$\mu\text{A}$
Input Leakage Current (PWRDWN, ALSB)	$I_{IN}$		-10		+48	$\mu\text{A}$
Input Capacitance	$C_{IN}$				10	pF
DIGITAL OUTPUTS						
Output High Voltage (DVDDIO = 3.3 V)	$V_{OH}$	$I_{SOURCE} = 0.4\text{ mA}$	2.4			V
Output High Voltage (DVDDIO = 1.8 V)	$V_{OH}$	$I_{SOURCE} = 0.4\text{ mA}$	1.4			V
Output Low Voltage (DVDDIO = 3.3 V)	$V_{OL}$	$I_{SINK} = 3.2\text{ mA}$			0.4	V
Output Low Voltage (DVDDIO = 1.8 V)	$V_{OL}$	$I_{SINK} = 1.6\text{ mA}$			0.2	V
High Impedance Leakage Current	$I_{LEAK}$				10	$\mu\text{A}$
Output Capacitance	$C_{OUT}$				20	pF
POWER REQUIREMENTS <sup>1, 2</sup>						
Digital I/O Power Supply	$D_{VDDIO}$		1.71	3.3	3.46	V
PLL Power Supply	$P_{VDD}$		1.71	1.8	1.89	V
Analog Power Supply	$A_{VDD}$		1.71	1.8	1.89	V
Digital Power Supply	$D_{VDD}$		1.71	1.8	1.89	V
Digital I/O Supply Current	$I_{DVDDIO}$			3		mA
PLL Supply Current	$I_{PVDD}$			12		mA
Analog Supply Current	$I_{AVDD}$	Single-ended CVBS input		35		mA
		Differential CVBS input		69		mA
		Single-ended CVBS fast switch		35		mA
		Differential CVBS fast switch		69		mA
		Y/C input		60		mA
		YPrPb input		75		mA
Digital Supply Current	$I_{DVDD}$	Single-ended CVBS input		60		mA
		Differential CVBS input		66		mA
		Single-ended CVBS fast switch		60		mA
		Differential CVBS fast switch		66		mA
		Y/C input		60		mA
		YPrPb input		60		mA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>POWER DOWN PERFORMANCE<sup>1</sup></b>						
Digital I/O Supply Power-Down Current	I <sub>DVDDIO</sub>			73		μA
PLL Supply Power-Down Current	I <sub>PVDD</sub>			38		μA
Analog Supply Power-Down Current	I <sub>AVDD</sub>			0.15		μA
Digital Supply Power-Down Current	I <sub>DVDD</sub>			368		μA
Total Power Dissipation in Power-Down Mode				1		mW

<sup>1</sup> Guaranteed by characterization.

<sup>2</sup> Typical current consumption values are recorded with nominal voltage supply levels and an SMPTEBAR test pattern.

## VIDEO SPECIFICATIONS

Guaranteed by characterization. A<sub>VDD</sub>, D<sub>VDD</sub>, and P<sub>VDD</sub> = 1.71 V to 1.89 V; D<sub>VDDIO</sub> = 1.71 V to 3.46 V, specified at operating temperature range, unless otherwise noted.

**Table 3.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>NONLINEAR SPECIFICATIONS<sup>1</sup></b>						
Differential Phase	DP	CVBS input, modulate five-step		0.9		Degrees
Differential Gain	DG	CVBS input, modulate five-step		0.5		%
Luma Nonlinearity	LNL	CVBS input, five-step		2.0		%
<b>NOISE SPECIFICATIONS</b>						
SNR Unweighted		Luma ramp		57		dB
		Luma flat field		58		dB
Analog Front-End Crosstalk				60		dB
Common-Mode Rejection <sup>2</sup>	CMR			75		dB
<b>LOCK TIME SPECIFICATIONS</b>						
Horizontal Lock Range			-5		+5	%
Vertical Lock Range			40		70	Hz
f <sub>SC</sub> Subcarrier Lock Range				±1.3		kHz
Color Lock-In Time				60		Lines
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed <sup>3</sup>				100		Lines
Fast Switch Speed <sup>4</sup>				100		ms
<b>LUMA SPECIFICATIONS</b>						
Luma Brightness Accuracy		CVBS, 1 V input		1		%
Luma Contrast Accuracy		CVBS, 1 V input		1		%

<sup>1</sup> These specifications apply for all CVBS input types (NTSC, PAL, SECAM) as well as for single-ended and differential CVBS inputs.

<sup>2</sup> The common-mode rejection (CMR) of this circuit design is critically dependent on the external resistor matching on its inputs. This measurement was performed with 0.1% tolerant resistors, a common-mode voltage of 1 V, and a common-mode frequency of 10 kHz.

<sup>3</sup> This is the time that it takes the ADV7182 to detect which video format is present at its input, for example, PAL I or NTSC M.

<sup>4</sup> This is the time that it takes the ADV7182 to switch from one (single-ended or differential) analog input to another, for example, switching from A<sub>IN1</sub> to A<sub>IN2</sub>.

**TIMING SPECIFICATIONS**

Guaranteed by characterization.  $A_{VDD}$ ,  $D_{VDD}$ , and  $P_{VDD} = 1.71\text{ V to }1.89\text{ V}$ ;  $D_{VDDIO} = 1.71\text{ V to }3.46\text{ V}$ , specified at operating temperature range, unless otherwise noted.

Table 4.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Nominal Frequency				28.63636		MHz
Frequency Stability					±50	ppm
I <sup>2</sup> C PORT						
SCLK Frequency					400	kHz
SCLK Minimum Pulse Width High	$t_1$		0.6			µs
SCLK Minimum Pulse Width Low	$t_2$		1.3			µs
Hold Time (Start Condition)	$t_3$		0.6			µs
Setup Time (Start Condition)	$t_4$		0.6			µs
SDATA Setup Time	$t_5$		100			ns
SCLK and SDATA Rise Times	$t_6$				300	ns
SCLK and SDATA Fall Times	$t_7$				300	ns
Setup Time for Stop Condition	$t_8$			0.6		µs
RESET FEATURE						
RESET Pulse Width			5			ms
CLOCK OUTPUTS						
LLC Mark Space Ratio	$t_9, t_{10}$		45:55		55:45	% duty cycle
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	$t_{11}$	Negative clock edge to start of valid data ( $t_{ACCESS} = t_{10} - t_{11}$ )			3.8	ns
	$t_{12}$	End of valid data to negative clock edge ( $t_{HOLD} = t_9 + t_{12}$ )			6.9	ns

**Timing Diagrams**

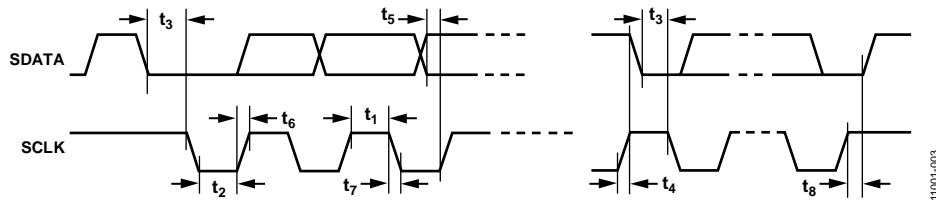


Figure 2. I<sup>2</sup>C Timing

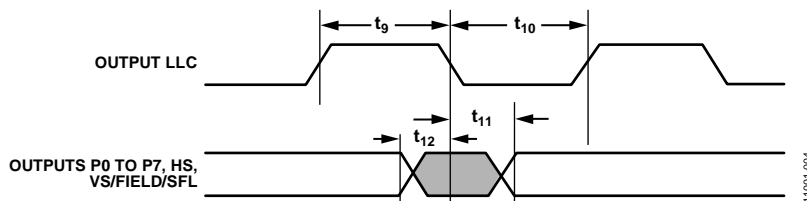


Figure 3. Pixel Port and Control Output Timing

**ANALOG SPECIFICATIONS**

Guaranteed by characterization.  $A_{VDD}$ ,  $D_{VDD}$ , and  $P_{VDD} = 1.71$  V to 1.89 V;  $D_{VDDIO} = 1.71$  V to 3.46 V, specified at operating temperature range, unless otherwise noted.

Table 5.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLAMP CIRCUITRY					
External Clamp Capacitor	Clamps switched off		0.1		$\mu$ F
Input Impedance			10		M $\Omega$
Large Clamp Source Current			0.32		mA
Large Clamp Sink Current			0.32		mA
Fine Clamp Source Current			7		$\mu$ A
Fine Clamp Sink Current			7		$\mu$ A

**THERMAL SPECIFICATIONS**

Table 6.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
THERMAL CHARACTERISTICS						
Junction-to-Ambient Thermal Resistance (Still Air)	$\theta_{JA}$	4-layer printed circuit board (PCB) with solid ground plane, 32-lead LFCSP		32.5		$^{\circ}$ C/W
Junction-to-Case Thermal Resistance	$\theta_{JC}$	4-layer PCB with solid ground plane, 32-lead LFCSP		2.3		$^{\circ}$ C/W



## ABSOLUTE MAXIMUM RATINGS

Table 7.

Parameter	Rating
AVDD to AGND	2.2 V
DVDD to DGND	2.2 V
PVDD to AGND	2.2 V
DVDDIO to DGND	4 V
DVDDIO to AVDD	-0.3 V to +4 V
PVDD to DVDD	-0.3 V to +0.9 V
DVDDIO to PVDD	-0.3 V to +4 V
DVDDIO to DVDD	-0.3 V to +4 V
AVDD to PVDD	-0.3 V to +0.3 V
AVDD to DVDD	-0.3 V to +0.9 V
Digital Inputs Voltage	DGND - 0.3 V to DVDDIO + 0.3 V
Digital Outputs Voltage	DGND - 0.3 V to DVDDIO + 0.3 V
Analog Inputs to AGND	AGND - 0.3 V to AVDD + 0.3 V
Maximum Junction Temperature (T <sub>j</sub> max)	140°C
Storage Temperature Range	-65°C to +150°C
Infrared Reflow Soldering (20 sec)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

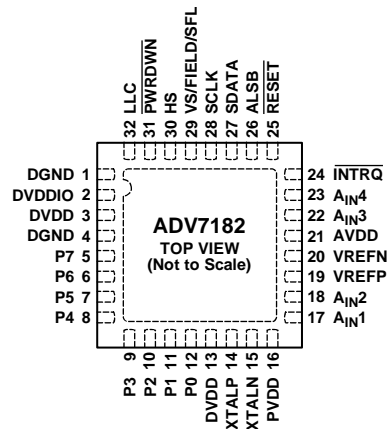
This device is a high performance integrated circuit with an ESD rating of <2 kV, and it is ESD sensitive. Proper precautions should be taken for handling and assembly.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES  
1. THE EXPOSED PAD MUST BE CONNECTED TO DGND.

Figure 4. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Type	Description
1, 4	DGND	G	Ground for Digital Supply.
2	DVDDIO	P	Digital I/O Supply Voltage (1.8 V to 3.3 V).
3, 13	DVDD	P	Digital Supply Voltage (1.8 V).
5 to 12	P7 to P0	O	Video Pixel Output Port.
14	XTALP	O	This pin should be connected to the 28.6363 MHz crystal or not connected if an external 1.8 V, 28.6363 MHz clock oscillator source is used to clock the <b>ADV7182</b> . In crystal mode, the crystal must be a fundamental crystal.
15	XTALN	I	Input Pin for the 28.6363 MHz Crystal. This pin can be overdriven by an external 1.8 V, 28.6363 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
16	PVDD	P	PLL Supply Voltage (1.8 V).
17, 18, 22, 23	A <sub>IN</sub> 1 to A <sub>IN</sub> 4	I	Analog Video Input Channels.
19	VREFP	O	Internal Voltage Reference Output.
20	VREFN	O	Internal Voltage Reference Output.
21	AVDD	P	Analog Supply Voltage (1.8 V).
24	INTRQ	O	Interrupt Request Output. Interrupt occurs when certain signals are detected on the input video.
25	RESET	I	System Reset Input. Active low. A minimum low reset pulse width of 5 ms is required to reset the <b>ADV7182</b> circuitry.
26	ALSB	I	This pin selects the I <sup>2</sup> C address for the <b>ADV7182</b> . For ALSB set to Logic 0, the address selected for a write is 0x40; for ALSB set to Logic 1, the address selected is 0x42.
27	SDATA	I/O	I <sup>2</sup> C Port Serial Data Input/Output Pin.
28	SCLK	I	I <sup>2</sup> C Port Serial Clock Input. The maximum clock rate is 400 kHz.
29	VS/FIELD/SFL	O	Vertical Synchronization Output Signal/Field Synchronization Output Signal/Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices digital video encoder.
30	HS	O	Horizontal Synchronization Output Signal.
31	PWRDWN	I	A logic low on this pin places the <b>ADV7182</b> in power-down mode.
32	LLC	O	Line-Locked Output Clock for Output Pixel Data. Nominally 27 MHz but varies up or down according to the video line length.
	EPAD (EP)		The exposed pad must be connected to DGND.

## POWER SUPPLY SEQUENCING

### POWER-UP SEQUENCE

The recommended power-up sequence of the [ADV7182](#) is

- 3.3 V supply (DVDDIO)
- 1.8 V supplies (DVDD, PVDD, AVDD)

Note the following:

- Power up the DVDDIO supply first. This is true regardless if DVDDIO is powered up to 3.3 V or 1.8 V.
- Power up the 1.8 V supplies only after DVDDIO has been fully asserted.
- Assert (pull low) the  $\overline{\text{PWRDWN}}$  and  $\overline{\text{RESET}}$  pins while the supplies are being powered up. A 5 ms reset operation is needed after power-up. See the Power-On  $\overline{\text{RESET}}$  section for further details.
- After all the power supplies and the  $\overline{\text{PWRDWN}}$  and  $\overline{\text{RESET}}$  pins are powered-up and stable, a further 5 ms delay is needed before I<sup>2</sup>C communication can be performed with the [ADV7182](#).
- During power-up, all supplies must adhere to the specifications listed in the Absolute Maximum Ratings section.

The [ADV7182](#) can be alternatively powered up by asserting all supplies simultaneously. In this case, care must be taken to ensure that a lower rated supply does not go above a higher rated supply level as the supplies are being established.

### POWER-ON $\overline{\text{RESET}}$

After power-up, it is necessary to execute a reset operation. For correct operation,  $\overline{\text{RESET}}$  should remain asserted (pulled low) for 5 ms after power supplies are stable and within specification, and  $\overline{\text{PWRDWN}}$  is deasserted (pulled high).

### POWER-DOWN SEQUENCE

The [ADV7182](#) supplies can be deasserted simultaneously as long as DVDDIO does not go below a lower rated supply.

### UNIVERSAL POWER SUPPLY

It is possible to power all the supplies (DVDD, PVDD, AVDD, and DVDDIO) to 1.8 V.

In this setup, note the following:

- Follow the power-up sequence described in the Power Supply Sequencing section. Power up the DVDDIO supply to 1.8 V instead of 3.3 V. Also, power up the  $\overline{\text{PWRDWN}}$  and  $\overline{\text{RESET}}$  pins to 1.8 V instead of 3.3 V.
- Set the drive strengths of the digital outputs of the [ADV7182](#) to their maximum setting. See the Global Pin Control section.
- Connect any pull-up resistors connected to pins on the [ADV7182](#) (such as the SCLK and SDATA pins) to 1.8 V and not 3.3 V.

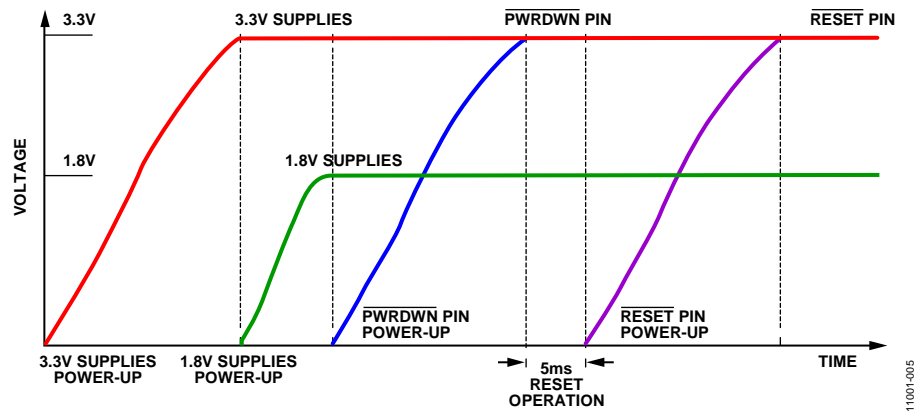


Figure 5. Recommended Power-Up Sequence

## INPUT NETWORKS

This section describes the input networks (external resistor and capacitor circuits) that should be placed on the analog video input ( $A_{IN}$ ) pins of the [ADV7182](#). Different input networks are required for different analog input video formats.

### SINGLE-ENDED INPUT NETWORK

Use the input network described in Figure 6 on each  $A_{IN}$  input pin of the [ADV7182](#) when any of the following video input formats are used: single-ended CVBS, YC (S-Video), or YPrPb.

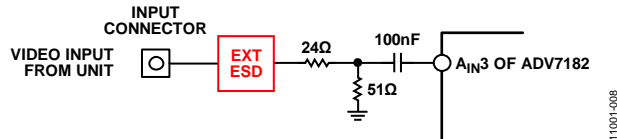


Figure 6. Input Single-Ended Network

The 24  $\Omega$  and 51  $\Omega$  resistors supply the 75  $\Omega$  end termination required for the analog video input. In addition, these resistors create a resistor divider with a 0.68 gain that attenuates the amplitude of the inputted analog video and scales the input to the ADC range of the [ADV7182](#). This allows the [ADV7182](#) to have an input range of up to 1.47 V p-p.

Note that amplifiers within the [ADV7182](#) restore the amplitude of the input signal so that signal-to-noise (SNR) performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the analog input pins of the [ADV7182](#).

The clamping circuitry within the [ADV7182](#) restores the dc bias of the input signal to the optimal level before it is fed into the ADC of the [ADV7182](#). See the Clamp Operation section for more information.

### DIFFERENTIAL INPUT NETWORK

Use the input network described in Figure 7 when differential CVBS video is input on the  $A_{IN}$  input pins of the [ADV7182](#).

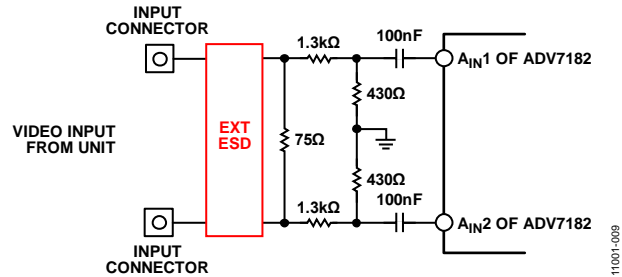


Figure 7. Input Differential Network

Differential video transmission involves transmitting two complementary CVBS signals. It has several key advantages over single-ended transmission, some of which include the following:

- Inherent small signal and large signal noise rejection
- Improved EMI performance
- Ability to absorb ground bounce

The 75  $\Omega$  resistor supplies the end termination required for the analog video input. Note that, if a 150  $\Omega$  termination is required, the 75  $\Omega$  resistor can be replaced with a 150  $\Omega$  resistor.

The 1.3 k $\Omega$  and 430  $\Omega$  resistors provide a resistor divider with a 0.25 gain. This results in an attenuation of the inputted analog video but also an increase in the input common-mode range of the [ADV7182](#) of up to 4 V p-p.

Note that amplifiers within the [ADV7182](#) restore the amplitude of the input signal so that SNR performance is maintained.

The 100 nF ac coupling capacitor removes the dc bias of the analog input video before it is fed into the analog video input pins of the [ADV7182](#).

The clamping circuitry within the [ADV7182](#) restores the dc bias of the optimized level before it is fed into the ADC of the [ADV7182](#). See the Clamp Operation section for further information.

The combination of the 1.3 k $\Omega$  and 430  $\Omega$  resistors and the 100 nF ac coupling capacitor limits current flow into the [ADV7182](#) during short-to-battery (STB) events.

To achieve optimal performance, closely match the 1.3 k $\Omega$  and 430  $\Omega$  resistors; that is, all the 1.3 k $\Omega$  and 430  $\Omega$  resistors should have the same resistance tolerance, and this tolerance should be as low as possible.

## ANALOG FRONT END

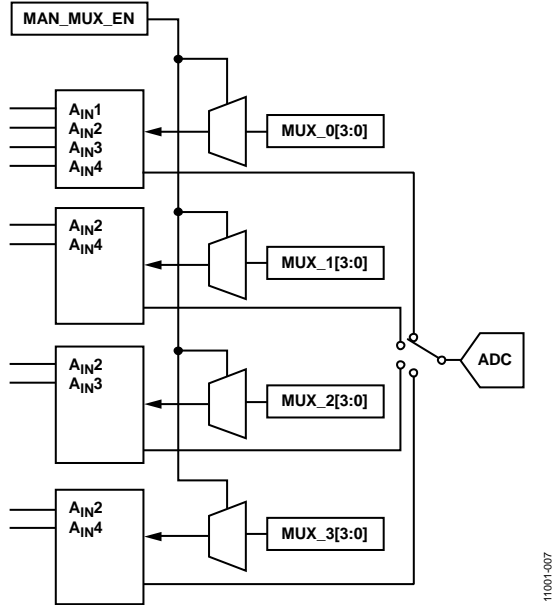


Figure 8. Manual Muxing

### INPUT CONFIGURATION

The following two steps are key for configuring the [ADV7182](#) to correctly decode the input video.

1. Use INSEL[4:0] to configure the routing and format decoding (CVBS, Y/C, or YPrPb).
2. If the input requirements are not met using the INSEL[4:0] options, the analog input muxing section must be configured manually to correctly route the video from the analog input pins to the ADC. The standard definition processor block, which decodes the digital data, should be configured to process the CVBS, Y/C, or YPrPb format. This is performed by INSEL[4:0] selection.

### INSEL[4:0], Input Control, Address 0x00[4:0]

The INSEL bits allow the user to select the input format. They also configure the standard definition processor core to process CVBS, differential CVBS, S-Video (Y/C), or component (YPrPb) format.

INSEL[4:0] has predefined analog input routing schemes that do not require manual mux programming (see Table 9). This allows the user to route the various video signal types to the decoder and select them using INSEL[4:0] only. The added benefit is that if, for example, the CVBS input is selected, the remaining channels are powered down.

Table 9. INSEL[4:0]

INSEL[4:0]	Video Format	Analog Input
00000	CVBS	CVBS input on A <sub>IN</sub> 1
00001	CVBS	CVBS input on A <sub>IN</sub> 2
00010	CVBS	CVBS input on A <sub>IN</sub> 3
00011	CVBS	CVBS input on A <sub>IN</sub> 4
01000	Y/C (S-Video)	Y input on A <sub>IN</sub> 1
		C input on A <sub>IN</sub> 2
01001	Y/C (S-Video)	Y input on A <sub>IN</sub> 3
		C input on A <sub>IN</sub> 4
01100	YPrPb	Y input on A <sub>IN</sub> 1
		Pb input on A <sub>IN</sub> 2
		Pr input on A <sub>IN</sub> 3
01110	Differential CVBS	Positive on A <sub>IN</sub> 1
		Negative on A <sub>IN</sub> 2
01111	Differential CVBS	Positive on A <sub>IN</sub> 3
		Negative on A <sub>IN</sub> 4

### ANALOG INPUT MUXING

The [ADV7182](#) has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder.

A maximum of four CVBS inputs can be connected to and decoded by the [ADV7182](#). As shown in the Pin Configuration and Function Description section, these analog input pins lie in close proximity to one another, which requires careful design of the PCB layout. For example, route ground shielding between all signals through tracks that are physically close together. It is strongly recommended that any unused analog input pins be connected to AGND to act as a shield.

**MAN\_MUX\_EN, Manual Input Muxing Enable, Address 0xC4[7]**

To configure the **ADV7182** analog muxing section, the user must select the analog input A<sub>IN</sub>1 to A<sub>IN</sub>8 that is to be processed by the ADC. MAN\_MUX\_EN must be set to 1 to enable the following muxing blocks:

- MUX0[2:0], ADC mux configuration, Address 0xC3[2:0]
- MUX1[2:0], ADC mux configuration, Address 0xC3[6:4]
- MUX2[2:0], ADC mux configuration, Address 0xC4[2:0]
- MUX3[2:0], ADC mux configuration, Address 0x60[2:0]

The four mux sections are controlled by the signal buses, MUX0/MUX1/MUX2/MUX3[2:0]. Table 10 explains the control words used.

The input signal that contains the timing information (HS and VS) must be processed by MUX0. For example, in a Y/C input configuration, connect MUX0 to the Y channel and MUX1 to the C channel. When one or more muxes are not used to process video, such as the CVBS input, the idle mux and associated channel clamps and buffers should be powered down (see the description of Register 0x3A in Table 94).

**Table 10. Manual Mux Settings for ADC (MAN\_MUX\_EN Must be Set to 1)**

<b>MUX0[2:0]</b>	<b>ADC Connected To</b>	<b>MUX1[2:0]</b>	<b>ADC Connected To</b>	<b>MUX2[2:0]</b>	<b>ADC Connected To</b>	<b>MUX3[2:0]</b>	<b>ADC Connected To</b>
000	No connect	000	No connect	000	No connect	000	No connect
001	A <sub>IN</sub> 1	001	No connect	001	No connect	001	No connect
010	A <sub>IN</sub> 2	010	A <sub>IN</sub> 2	010	A <sub>IN</sub> 2	010	A <sub>IN</sub> 2
011	A <sub>IN</sub> 3	011	No connect	011	A <sub>IN</sub> 3	011	No connect
100	A <sub>IN</sub> 4	100	A <sub>IN</sub> 4	100	No connect	100	A <sub>IN</sub> 4

**Notes:**

- CVBS can only be processed by MUX0.
- Differential CVBS can only be processed by MUX0 (positive channel) and MUX3 (negative channel).
- Y/C can only be processed by MUX0 and MUX1.
- YPrPb can only be processed by MUX0, MUX1, and MUX2.

**ANTI\_ALIASING FILTERS**

The ADV7182 has optional on-chip antialiasing (AA) filters on each of the four channels that are multiplexed to the ADC (see Figure 9). The filters are designed for standard definition video up to 10 MHz bandwidth. Figure 10 and Figure 11 show the filter magnitude and phase characteristics.

The antialiasing filters are enabled by default and the selection of INSEL[4:0] determines which filters are powered up at any given time. For example, if CVBS mode is selected, the filter circuits for the remaining input channels are powered down to conserve power. However, the antialiasing filters can be disabled or bypassed using the AA\_FILT\_MAN\_OVR control.

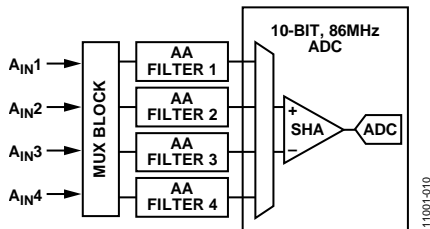


Figure 9. Antialias Filter Configuration

**AA\_FILT\_MAN\_OVR, Antialiasing Filter Override, Address 0xF3[4]**

This feature allows the user to override the antialiasing filters on/off settings, which are automatically selected by INSEL[4:0].

**AA\_FILT\_EN[3:0], Antialiasing Filter Enable, Address 0xF3[3:0]**

These bits allow the user to enable or disable the antialiasing filters on each of the three input channels multiplexed to the ADC. When disabled, the analog signal bypasses the AA filters and is routed directly to the ADC.

**AA\_FILT\_EN[0], Antialiasing Filter Enable, Address 0xF3[0]**

When AA\_FILT\_EN[0] is 0, AA Filter 1 is disabled.

When AA\_FILT\_EN[0] is 1, AA Filter 1 is enabled.

**AA\_FILT\_EN[1], Antialiasing Filter Enable, Address 0xF3[1]**

When AA\_FILT\_EN[1] is 0, AA Filter 2 is disabled.

When AA\_FILT\_EN[1] is 1, AA Filter 2 is enabled.

**AA\_FILT\_EN[2], Antialiasing Filter Enable, Address 0xF3[2]**

When AA\_FILT\_EN[2] is 0, AA Filter 3 is disabled.

When AA\_FILT\_EN[2] is 1, AA Filter 3 is enabled.

**AA\_FILT\_EN[3], Antialiasing Filter Enable, Address 0xF3[3]**

When AA\_FILT\_EN[3] is 0, AA Filter 4 is disabled.

When AA\_FILT\_EN[3] is 1, AA Filter 4 is enabled.

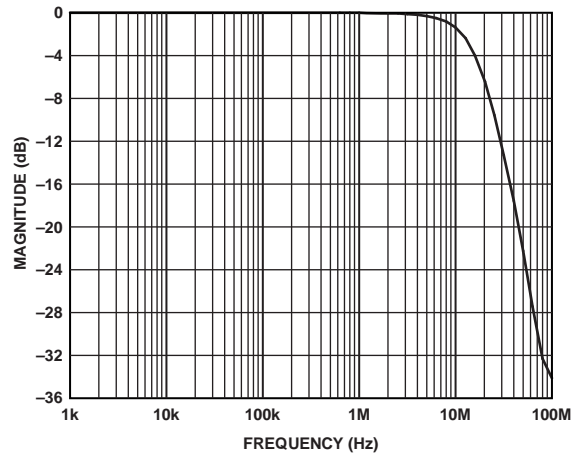


Figure 10. Antialiasing Filter Magnitude Response

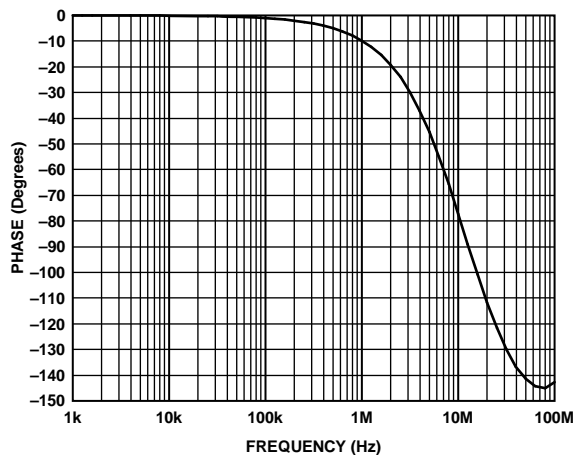


Figure 11. Antialiasing Filter Phase Response

## GLOBAL CONTROL REGISTERS

Register control bits listed in this section affect the whole chip.

### POWER-SAVING MODES

#### **Power-Down**

##### **PWRDWN, Address 0x0F[5]**

The [ADV7182](#) can be placed into a chip-wide, power-down mode by setting the PWRDWN bit or by using the  $\overline{\text{PWRDWN}}$  pin.

The power-down mode stops the clock from entering the digital section of the chip, thereby freezing its operation. No I<sup>2</sup>C bits are lost during power-down mode. The PWRDWN bit also affects the analog blocks and switches them into low current modes. The I<sup>2</sup>C interface is unaffected and remains operational in power-down mode.

When PWRDWN is 0, the chip is operational. When PWRDWN is 1 (default), the [ADV7182](#) is in a chip-wide, power-down mode.

### RESET CONTROL

#### **Reset, Chip Reset, Address 0x0F[7]**

Setting this bit, which is equivalent to controlling the  $\overline{\text{RESET}}$  pin on the [ADV7182](#), issues a full chip reset. All I<sup>2</sup>C registers are reset to their default/power-up values. Note that some register bits do not have a reset value specified. They keep their last written value. Those bits are marked as having a reset value of x in the register tables (see Table 94 and Table 96). After the reset sequence, the part immediately starts to acquire the incoming video signal.

After setting the reset bit (or initiating a reset via the  $\overline{\text{RESET}}$  pin), the part returns to the default for its primary mode of operation. All I<sup>2</sup>C bits are loaded with their default values, making this bit self-clearing. Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I<sup>2</sup>C writes are performed.

The I<sup>2</sup>C master controller receives a no acknowledge condition on the ninth clock cycle when chip reset is implemented (see the MPU Port Description section).

When the reset bit is 0 (default), operation is normal.

When the reset bit is 1, the reset sequence starts.

### GLOBAL PIN CONTROL

#### **Tristate Output Drivers**

##### **TOD, Address 0x03[6]**

This bit allows the user to tristate the output drivers of the [ADV7182](#).

Upon setting the TOD bit, the P7 to P0, HS, and VS/FIELD/SFL pins are tristated.

The timing pins (HS and VS/FIELD/SFL pins) can be forced active via the TIM\_OE bit. For more information on tristate control, see the Tristate LLC Driver and the Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR\_STR\_x bits.

When TOD is 0 (default), the output drivers are enabled.

When TOD is 1, the output drivers are tristated.

#### **Tristate LLC Driver**

##### **TRI\_LLC, Address 0x1D[7]**

This bit allows the output drivers for the LLC pin of the [ADV7182](#) to be tristated. For more information on tristate control, refer to the Tristate Output Drivers and Timing Signals Output Enable sections.

Individual drive strength controls are provided via the DR\_STR\_x bits.

When TRI\_LLC is 0 (default), the LLC pin drivers work according to the DR\_STR\_C[1:0] setting (pin enabled).

When TRI\_LLC is 1, the LLC pin drivers are tristated.

#### **Timing Signals Output Enable**

##### **TIM\_OE, Address 0x04[3]**

The TIM\_OE bit should be regarded as an addition to the TOD bit. Setting it high forces the output drivers for HS, VS/FIELD/SFL into the active state (that is, driving state) even if the TOD bit is set. If TIM\_OE is set to low, the HS and VS/FIELD/SFL pins are tristated depending on the TOD bit. This functionality is beneficial if the decoder is used only as a timing generator. This may be the case if only the timing signals are extracted from an incoming signal or if the part is in free-run mode, where a separate chip can output a company logo, for example.

For more information on tristate control, see the Tristate Output Drivers and Tristate LLC Driver sections.

Individual drive strength controls are provided via the DR\_STR\_x bits.

When TIM\_OE is 0 (default), HS and VS/FIELD/SFL are tristated according to the TOD bit.

When TIM\_OE is 1, HS and VS/FIELD/SFL are forced active all the time.



**VS/FIELD/SFL Sync Mux Selection****FLD\_OUT\_SEL[2:0], Address 0x6B[2:0]**

The FLD\_OUT\_SEL[2:0] bits select whether the VS/FIELD/SFL pin outputs vertical sync, horizontal sync, field sync, data enable (DE), or subcarrier frequency lock (SFL) signals.

Note that the VS/FIELD/SFL pin must be active for this selection to occur. See the Tristate Output Drivers and Tristate LLC Driver sections.

**Table 11. FLD\_OUT\_SEL Function**

FLD_OUT_SEL[2:0]	Description
000	The VS/FIELD/SFL pin outputs horizontal sync information.
001	The VS/FIELD/SFL pin outputs vertical sync information.
010 (default)	The VS/FIELD/SFL pin outputs field sync information.
011	The VS/FIELD/SFL pin outputs data enable (DE) information.
100	The VS/FIELD/SFL pin outputs subcarrier frequency lock information.

**HS Sync Mux Selection****HS\_OUT\_SEL[2:0], Address 0x6A[2:0]**

The HS\_OUT\_SEL[2:0] bits allow the user to change the operation of the HS pin. The HS pin is set to output horizontal sync signals as the default. The user can also set the HS pin to output vertical sync, field sync, data enable (DE), or subcarrier frequency lock (SFL) information.

Note that the HS pin must be active for this selection to occur. See the Tristate Output Drivers and Tristate LLC Driver sections.

**Table 12. HS\_OUT\_SEL Function**

HS_OUT_SEL[2:0]	Description
000 (default)	The HS pin output horizontal sync information.
001	The HS pin outputs vertical sync information.
010	The HS pin outputs field sync information.
011	The HS pin outputs data enable (DE) information.
100	The HS pin outputs subcarrier frequency lock (SFL) information.

**Drive Strength Selection (Data)****DR\_STR[1:0], Address 0xF4[5:4]**

For EMC and crosstalk reasons, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR\_STR[1:0] bits affect the drive strength for the pixel output pins (P[7:0]) and the timing pins (HS and VS/FIELD/SFL).

For more information on tristate control, see the Tristate Output Drivers and Tristate LLC Driver sections.

**Table 13. DR\_STR Function**

DR_STR[1:0]	Description
00	Low drive strength (1x)
01 (default)	Medium low drive strength (2x)
10	Medium high drive strength (3x)
11	High drive strength (4x)

**Drive Strength Selection (Clock)****DR\_STR\_C[1:0], Address 0xF4[3:2]**

The DR\_STR\_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, see the Drive Strength Selection (Data) Section.

**Table 14. DR\_STR\_C Function**

DR_STR_C[1:0]	Description
00	Low drive strength (1x)
01 (default)	Medium low drive strength (2x)
10	Medium high drive strength (3x)
11	High drive strength (4x)

**Drive Strength Selection (I<sup>2</sup>C)****DR\_STR\_S[1:0], Address 0xF4[1:0]**

The DR\_STR\_S[1:0] bits allow the user to select the strength of the I<sup>2</sup>C signal output drivers. This affects the drive strength for the SDA and SCL pins.

**Table 15. DR\_STR\_S Function**

DR_STR_S[1:0]	Description
00	Low drive strength (1x)
01 (default)	Medium low drive strength (2x)
10	Medium high drive strength (3x)
11	High drive strength (4x)

**Enable Subcarrier Frequency Lock Pin****EN\_SFL\_PIN, Address 0x04[1]**

The EN\_SFL\_PIN bit enables the output of subcarrier lock information (also known as genlock) from the ADV7182 core to an encoder in a decoder/encoder back-to-back arrangement.

When the EN\_SFL\_PIN is 0 (default), the subcarrier frequency lock output is disabled.

When EN\_SFL\_PIN is 1, the subcarrier frequency lock information is presented on the SFL pin.

**Polarity LLC Pin****PCLK, Address 0x37[0]**

The polarity of the clock that leaves the ADV7182 via the LLC pin can be inverted using the PCLK bit. Changing the polarity of the LLC clock output may be necessary to meet the setup-and-hold time expectations of follow-on chips. When PCLK is 0, the LLC output polarity is inverted. When PCLK is 1 (default), the LLC output polarity is normal (see the Timing Specifications section).

## GLOBAL STATUS REGISTER

Four registers provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the [ADV7182](#). The other three registers (Address 0x10, Address 0x12, and Address 0x13) contain status bits from the [ADV7182](#).

### IDENTIFICATION

#### IDENT[7:0], Address 0x11[7:0]

This is the register identification of the [ADV7182](#) revision. Table 16 describes the various versions of the [ADV7182](#).

Table 16. IDENT CODE

IDENT[7:0]	Description
0x40	Initial release silicon
0x41	1 <sup>st</sup> revision of silicon

### STATUS 1

#### Status 1[7:0], Address 0x10[7:0]

This read-only register provides information about the internal status of the [ADV7182](#).

See the CIL[2:0], Count into Lock, Address 0x51[2:0] section and the COL[2:0], Count out of Lock, Address 0x51[5:3] section for details on timing.

Depending on the setting of the FSCLE bit, the status registers are based solely on horizontal timing information or on the horizontal timing and lock status of the color subcarrier. See the FSCLE, fSC Lock Enable, Address 0x51[7] section.

Table 17. Status 1 Function

Status 1[7:0]	Bit Name	Description
0	IN_LOCK	In lock (now)
1	LOST_LOCK	Lost lock (since last read)
2	FSC_LOCK	f <sub>SC</sub> locked (now)
3	FOLLOW_PW	AGC follows peak white algorithm
4	AD_RESULT[0]	Result of autodetection
5	AD_RESULT[1]	Result of autodetection
6	AD_RESULT[2]	Result of autodetection
7	COL_KILL	Color kill active

### STATUS 2

#### Status 2[7:0], Address 0x12[7:0]

Table 18. Status 2 Function

Status 2[7:0]	Bit Name	Description
0	MVCS_DET	Detected Macrovision color striping
1	MVCS_T3	Macrovision color striping protection; conforms to Type 3 if high, Type 2 if low
2	MV_PS_DET	Detected Macrovision pseudo-sync pulses
3	MV_AGC_DET	Detected Macrovision AGC pulses
4	LL_NSTD	Line length is nonstandard
5	FSC_NSTD	f <sub>SC</sub> frequency is nonstandard
6	Reserved	
7	Reserved	

### STATUS 3

#### Status 3[7:0], Address 0x13[7:0]

Table 19. Status 3 Function

Status 3[7:0]	Bit Name	Description
0	INST_HLOCK	Horizontal lock indicator (instantaneous)
1	Reserved	
2	SD_OP_50Hz	Flags whether 50 Hz or 60 Hz is present at output
3	Reserved	Reserved
4	FREE_RUN_ACT	Flags if <a href="#">ADV7182</a> has entered free-run mode (see Free-Run Operation section)
5	STD_FLD_LEN	Field length is correct for currently selected video standard
6	Interlaced	Interlaced video detected (field sequence found)
7	PAL_SW_LOCK	Reliable sequence of swinging bursts detected

### AUTODETECTION RESULT

#### AD\_RESULT[2:0], Address 0x10[6:4]

The AD\_RESULT[2:0] bits report back on the findings from the [ADV7182](#) autodetection block. See the General Setup section for more information on enabling the autodetection block and the Autodetection of SD Modes section for more information on how to configure it.

Table 20. AD\_RESULT Function

AD_RESULT[2:0]	Description
000	NTSC M/NTSC J
001	NTSC 4.43
010	PAL M
011	PAL 60
100	PAL B/PAL G/PAL H/PAL I/PAL D
101	SECAM
110	PAL Combination N
111	SECAM 525

## VIDEO PROCESSOR

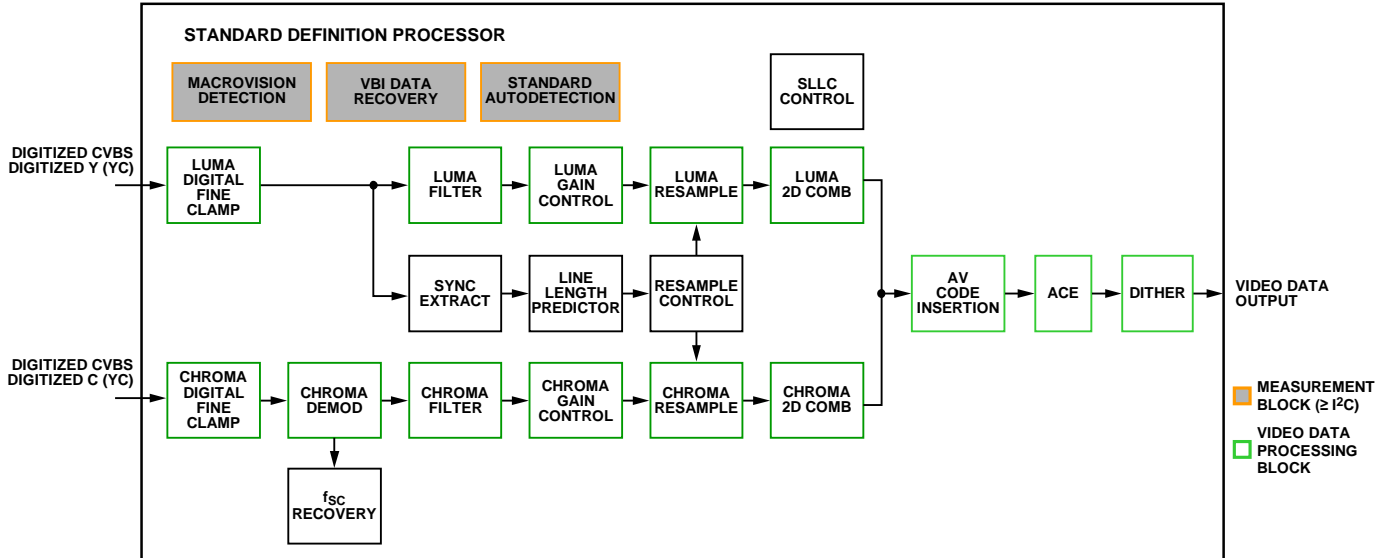


Figure 12. Block Diagram of Video Processor

Figure 12 shows a block diagram of the [ADV7182](#) video processor. The [ADV7182](#) can handle standard definition video in CVBS, Y/C, and YPrPb formats. It can be divided into a luminance and chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input.

### SD LUMA PATH

The input signal is processed by the following blocks:

- Luma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma filter. This block contains a luma decimation filter (YAA) with a fixed response and some shaping filters (YSH) that have selectable responses.
- Luma gain control. The AGC can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma resample. To correct for line length errors as well as dynamic line length changes, the data is digitally resampled.
- Luma 2D comb. The 2D comb filter provides Y/C separation.
- AV code insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes can be inserted (as per ITU-R BT.656).

### SD CHROMA PATH

The input signal is processed by the following blocks:

- Chroma digital fine clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma demodulation. This block employs a color subcarrier ( $f_{sc}$ ) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC, and an FM demodulation for SECAM.
- Chroma filter. This block contains a chroma decimation filter (CAA) with a fixed response and some shaping filters (CSH) that have selectable responses.
- Chroma gain control. AGC can operate on several different modes, including gain based on the color subcarrier amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is done to correct for static and dynamic line length errors of the incoming video signal.
- Chroma 2D comb. The 2D, five line, superadaptive comb filter provides high quality Y/C separation in case the input signal is CVBS.
- AV code insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes can be inserted (as per ITU-R BT.656).

## ACE AND DITHER PROCESSING BLOCKS

- ACE. This block offers improved visual detail by using an algorithm to automatically vary the contrast levels to enhance picture detail. See the Adaptive Contrast Enhancement section.
- Dither. When enabled, this block converts the digital output of the ADV7182 from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the ADV7182 to communicate with some LCD panels. See the Dither Function section.

## SYNC PROCESSING

The ADV7182 extracts syncs embedded in the analog input video signal. There is currently no support for external HS/VS inputs. The sync extraction is optimized to support imperfect video sources, such as VCRs with head switches. The actual algorithm used employs a coarse detection based on a threshold crossing, followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line length measurement and prediction block. The output of this is then used to drive the digital resampling section to ensure that the ADV7182 outputs 720 active pixels per line.

The sync processing on the ADV7182 also includes the following specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video:

- VSync processor. This block provides extra filtering of the detected VSyncs to improve vertical lock.
- HSync processor. The HSync processor is designed to filter incoming HSyncs that were corrupted by noise, providing much improved performance for video signals with a stable time base but poor SNR.

## VBI DATA RECOVERY

The ADV7182 can retrieve the following information from the input video:

- Wide screen signaling (WSS)
- Copy generation management system (CGMS)
- Closed captioning (CCAP)
- Macrovision protection presence
- Teletext

The ADV7182 is also capable of automatically detecting the incoming video standard with respect to the following:

- Color subcarrier frequency
- Field rate
- Line rate

The ADV7182 can configure itself to support PAL B/PAL D/ PAL I/PAL G/PAL H, PAL M, PAL N, PAL Combination N, NTSC M/NTSC J, SECAM 50 Hz/60 Hz, NTSC 4.43, and PAL 60.

## GENERAL SETUP

### Video Standard Selection

The VID\_SEL[3:0] bits (Address 0x02[7:4]) allow the user to force the digital core into a specific video standard. This is not necessary under normal circumstances. The VID\_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and variants thereof.

### Autodetection of SD Modes

To guide the autodetect system of the ADV7182, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system chooses the closest of the remaining enabled standards. The results of the autodetection block can be read back via the status registers (see the Global Status Register section for more information).

VID\_SEL[3:0], Address 0x02[7:4]

Table 21. VID\_SEL Function

VID_SEL[3:0]	Description
0000 (default)	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC J (no pedestal), SECAM
0001	Autodetect PAL B/PAL G/PAL H/PAL I/PAL D, NTSC M (pedestal), SECAM
0010	Autodetect PAL N (pedestal), NTSC J (no pedestal), SECAM
0011	Autodetect PAL N (pedestal), NTSC M (pedestal), SECAM
0100	NTSC J
0101	NTSC M
0110	PAL 60
0111	NTSC 4.43
1000	PAL B/PAL G/PAL H/PAL I/PAL D
1001	PAL N = PAL B/PAL G/PAL H/PAL I/PAL D (with pedestal)
1010	PAL M (without pedestal)
1011	PAL M
1100	PAL Combination N
1101	PAL Combination N (with pedestal)
1110	SECAM
1111	SECAM

### AD\_SEC525\_EN, SECAM 525 Autodetect Enable, Address 0x07[7]

Setting AD\_SEC525\_EN to 0 (default) disables the autodetection of a 525-line system with a SECAM style, FM-modulated color component.

Setting AD\_SEC525\_EN to 1 enables the detection of a SECAM style, FM-modulated color component.

**AD\_SECAM\_EN, SECAM Autodetect Enable,  
Address 0x07[6]**

Setting AD\_SECAM\_EN to 0 (default) disables the autodetection of SECAM.

Setting AD\_SECAM\_EN to 1 enables the detection of SECAM.

**AD\_N443\_EN, NTSC 4.43 Autodetect Enable,  
Address 0x07[5]**

Setting AD\_N443\_EN to 0 disables the autodetection of NTSC style systems with a 4.43 MHz color subcarrier.

Setting AD\_N443\_EN to 1 (default) enables the detection of NTSC style systems with a 4.43 MHz color subcarrier.

**AD\_P60\_EN, PAL 60 Autodetect Enable, Address 0x07[4]**

Setting AD\_P60\_EN to 0 disables the autodetection of PAL systems with a 60 Hz field rate.

Setting AD\_P60\_EN to 1 (default) enables the detection of PAL systems with a 60 Hz field rate.

**AD\_PALN\_EN, PAL N Autodetect Enable,  
Address 0x07[3]**

Setting AD\_PALN\_EN to 0 (default) disables the detection of the PAL N standard.

Setting AD\_PALN\_EN to 1 enables the detection of the PAL N standard.

**AD\_PALM\_EN, PAL M Autodetect Enable,  
Address 0x07[2]**

Setting AD\_PALM\_EN to 0 (default) disables the autodetection of PAL M.

Setting AD\_PALM\_EN to 1 enables the detection of PAL M.

**AD\_NTSC\_EN, NTSC Autodetect Enable,  
Address 0x07[1]**

Setting AD\_NTSC\_EN to 0 (default) disables the detection of standard NTSC.

Setting AD\_NTSC\_EN to 1 enables the detection of standard NTSC.

**AD\_PAL\_EN, PAL B/PAL D/PAL I/PAL G/PAL H  
Autodetect Enable, Address 0x07[0]**

Setting AD\_PAL\_EN to 0 (default) disables the detection of standard PAL.

Setting AD\_PAL\_EN to 1 enables the detection of standard PAL.

**SFL\_INV, Subcarrier Frequency Lock Inversion,  
Address 0x41[6]**

This bit controls the behavior of the PAL switch bit in the SFL (genlock telegram) data stream. It was implemented to solve some compatibility issues with video encoders. It solves two problems.

First, the PAL switch bit is meaningful only in PAL. Some encoders (including Analog Devices encoders) also look at the state of this bit in NTSC.

Second, there was a design change in Analog Devices encoders from ADV717x to ADV719x. The older versions used the SFL (genlock telegram) bit directly, whereas the newer ones invert the bit prior to using it. The reason for this is that the inversion compensated for the one line delay of an SFL (genlock telegram) transmission.

As a result, for the ADV717x and ADV73xx encoders, the PAL switch bit in the SFL (genlock telegram) must be set to 0 for NTSC to work. For the older video encoders, the PAL switch bit in the SFL must be set to 1 to work in NTSC. If the state of the PAL switch bit is wrong, a 180° phase shift occurs.

In a decoder/encoder back-to-back system in which SFL is used, this bit must be set up properly for the specific encoder used.

Setting SFL\_INV to 0 (default) makes the part SFL compatible with the ADV717x and ADV73xx video encoders.

Setting SFL\_INV to 1 makes the part SFL compatible with the older video encoders.

**Lock Related Controls**

Lock information is presented to the user through Bits[2:0] of the Status 1 register (see the Status 1[7:0], Address 0x10[7:0] section). Figure 13 outlines the signal flow and the controls that are available to influence the way the lock status information is generated.

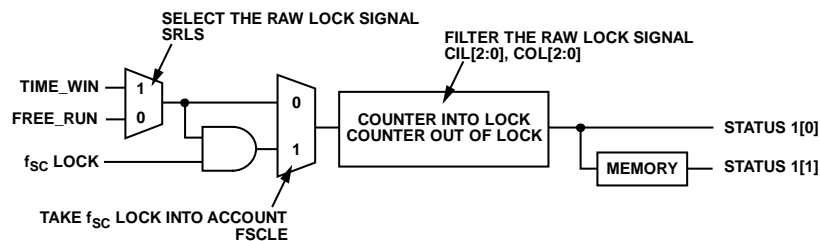


Figure 13. Lock Related Signal Path

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**SRLS, Select Raw Lock Signal, Address 0x51[6]**

Using the SRLS bit, the user can choose between two sources for determining the lock status (per Bits[1:0] in the Status 1 register). See Figure 13.

- The TIME\_WIN signal is based on a line-to-line evaluation of the horizontal synchronization pulse of the incoming video. It reacts quite quickly.
- The FREE\_RUN signal evaluates the properties of the incoming video over several fields, taking vertical synchronization information into account.

Setting SRLS to 0 (default) selects the FREE\_RUN signal (that is, evaluate over several fields).

Setting SRLS to 1 selects the TIME\_WIN signal (that is, evaluate on a line-to-line basis).

**FSCLE, f<sub>sc</sub> Lock Enable, Address 0x51[7]**

The FSCLE bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits[1:0] in the Status 1 register. This bit must be set to 0 when operating the ADV7182 in YPrPb component mode to generate a reliable HLOCK status bit.

When FSCLE is 0 (default), the overall lock status is dependent only on horizontal sync lock.

When FSCLE is 1, the overall lock status is dependent on horizontal sync lock and f<sub>sc</sub> lock.

**CIL[2:0], Count into Lock, Address 0x51[2:0]**

CIL[2:0] determines the number of consecutive lines for which the lock condition must be true before the system switches into the locked state and reports this via Status 1[1:0]. The bit counts the value in lines of video.

**Table 22. CIL Function**

CIL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

**COL[2:0], Count out of Lock, Address 0x51[5:3]**

COL[2:0] determines the number of consecutive lines for which the out-of-lock condition must be true before the system switches into the unlocked state and reports this via Status 1[1:0]. It counts the value in lines of video.

**Table 23. COL Function**

COL[2:0]	Number of Video Lines
000	1
001	2
010	5
011	10
100 (default)	100
101	500
110	1000
111	100,000

**COLOR CONTROLS**

These registers allow the user to control picture appearance, including control of active data in the event of video being lost. These controls are independent of any other controls. For instance, brightness control is independent of picture clamping, although both controls affect the dc level of the signal.

**CON[7:0], Contrast Adjust, Address 0x08[7:0]**

This register allows the user to control contrast adjustment of the picture.

**Table 24. CON Function**

CON[7:0]	Description
0x80 (default)	Gain on luma channel = 1
0x00	Gain on luma channel = 0
0xFF	Gain on luma channel = 2

**SD\_SAT\_Cb[7:0], SD Saturation Cb Channel, Address 0xE3[7:0]**

This register allows the user to control the gain of the Cb channel only, which in turn adjusts the saturation of the picture.

**Table 25. SD\_SAT\_Cb Function**

SD_SAT_Cb[7:0]	Description
0x80 (default)	Gain on Cb channel = 0 dB
0x00	Gain on Cb channel = -42 dB
0xFF	Gain on Cb channel = +6 dB

### SD\_SAT\_Cr[7:0], SD Saturation Cr Channel, Address 0xE4[7:0]

This register allows the user to control the gain of the Cr channel only, which in turn adjusts the saturation of the picture.

**Table 26. SD\_SAT\_Cr Function**

SD_SAT_Cr[7:0]	Description
0x80 (default)	Gain on Cr channel = 0 dB
0x00	Gain on Cr channel = -42 dB
0xFF	Gain on Cr channel = +6 dB

### SD\_OFF\_Cb[7:0], SD Offset Cb Channel, Address 0xE1[7:0]

This register allows the user to select an offset for the Cb channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register (Address 0X0B).

**Table 27. SD\_OFF\_Cb Function**

SD_OFF_Cb[7:0]	Description
0x80 (default)	0 mV offset applied to the Cb channel
0x00	-312 mV offset applied to the Cb channel
0xFF	+312 mV offset applied to the Cb channel

### SD\_OFF\_Cr[7:0], SD Offset Cr Channel, Address 0xE2[7:0]

This register allows the user to select an offset for the Cr channel only and to adjust the hue of the picture. There is a functional overlap with the HUE[7:0] register.

**Table 28. SD\_OFF\_Cr Function**

SD_OFF_Cr[7:0]	Description
0x80 (default)	0 mV offset applied to the Cr channel
0x00	-312 mV offset applied to the Cr channel
0xFF	+312 mV offset applied to the Cr channel

### BRI[7:0], Brightness Adjust, Address 0x0A[7:0]

This register controls the brightness of the video signal. It allows the user to adjust the brightness of the picture.

**Table 29. BRI Function**

BRI[7:0]	Description
0x00 (default)	Offset of the luma channel = 0 IRE
0x7F	Offset of the luma channel = +30 IRE
0x80	Offset of the luma channel = -30 IRE

### HUE[7:0], Hue Adjust, Address 0x0B[7:0]

This register contains the value for the color hue adjustment. It allows the user to adjust the hue of the picture.

HUE[7:0] has a range of  $\pm 90^\circ$ , with 0x00 equivalent to an adjustment of  $0^\circ$ . The resolution of HUE[7:0] is 1 bit =  $0.7^\circ$ .

The hue adjustment value is fed into the AM color demodulation block. Therefore, it applies only to video signals that contain chroma information in the form of an AM-modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video inputs (YPrPb).

**Table 30. HUE Function**

HUE[7:0]	Description (Adjust Hue of the Picture)
0x00 (default)	Phase of the chroma signal = $0^\circ$
0x7F	Phase of the chroma signal = $-90^\circ$
0x80	Phase of the chroma signal = $+90^\circ$

### DEF\_Y[5:0], Default Value Y, Address 0x0C[7:2]

When the ADV7182 loses lock on the incoming video signal or when there is no input signal, the DEF\_Y[5:0] register allows the user to specify a default luma value to be output. This value is used under the following conditions:

- If the DEF\_VAL\_AUTO\_EN bit is 1 and the ADV7182 has lost lock to the input video signal, this is the intended mode of operation (automatic mode).
- If the DEF\_VAL\_EN bit is 1, regardless of the lock status of the video decoder, this is a forced mode that may be useful during configuration.

The DEF\_Y[5:0] values define the six MSBs of the output video. The remaining LSBs are padded with 0s. For example, in 8-bit mode, the output is  $Y[7:0] = \{\text{DEF\_Y}[5:0], 0, 0\}$ .

For DEF\_Y[5:0], 0x0D (blue) is the default value for Y.

Register 0x0C has a default value of 0x36.

### DEF\_C[7:0], Default Value C, Address 0x0D[7:0]

The DEF\_C[7:0] register complements the DEF\_Y[5:0] value. It defines the four MSBs of Cr and Cb values to be output if:

- The DEF\_VAL\_AUTO\_EN bit is set to high and the ADV7182 cannot lock to the input video (automatic mode).
- The DEF\_VAL\_EN bit is set to high (forced output).

The data that is finally output from the ADV7182 for the chroma side is  $\text{Cr}[4:0] = \{\text{DEF\_C}[7:4]\}$  and  $\text{Cb}[4:0] = \{\text{DEF\_C}[3:0]\}$ .

For DEF\_C[7:0], 0x7C (blue) is the default value for Cr and Cb.

**FREE-RUN OPERATION**

Free-run mode provides the user with a stable clock and predictable data if the input signal cannot be decoded; for example, if input video is not present.

The ADV7182 automatically enters free-run mode if the input signal cannot be decoded. The user can prevent this operation by setting the DEF\_VAL\_AUTO\_EN to 0. When the DEF\_VAL\_AUTO\_EN bit is 0, the ADV7182 outputs noise if it cannot decode the input video. It is recommended that the user keep DEF\_VAL\_AUTO\_EN set to 1.

The user can force free-run mode by setting the DEF\_VAL\_EN bit to 1. This can be a useful tool in debugging system level issues.

The user can specify which data is output in free-run mode with the FREE\_RUN\_PAT\_SEL bits. The following test patterns can be set using this function:

- Single color
- Color bars
- Boundary box

**Single Color Test Pattern**

In this mode, the ADV7182 device can be set to output the default luma and chroma data stored in DEF\_Y and DEF\_C (see the Color Controls section).

**Color Bars Test Pattern**

In this mode, the ADV7182 device outputs the 100% color bars pattern.

**Boundary Box Test Pattern**

In this mode, the ADV7182 device outputs a black screen with a 1-pixel depth white border (see Figure 14).

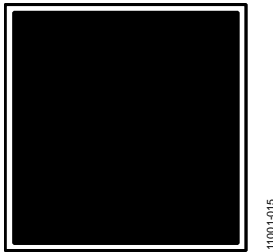


Figure 14. Boundary Box Free-Run Test Pattern

**DEF\_VAL\_AUTO\_EN, Default Value Automatic Enable, Address 0x0C[1]**

This bit enables the ADV7182 to enter free-run mode if it cannot decode the video signal that has been input.

Table 31. DEF\_VAL\_AUTO\_EN Function

DEF_VAL_AUTO_EN	Description
0	The ADV7182 outputs noise if it loses lock with the inputted video signal.
1 (default)	The ADV7182 enters free-run mode if it loses lock with the inputted video signal.

**DEF\_VAL\_EN, Default Value Enable, Address 0x0C[0]**

This bit forces free-run mode.

Table 32. DEF\_VAL\_EN Function

DEF_VAL_EN	Description
0 (default)	Do not force free-run mode (that is, free-run mode dependent on DEF_VAL_AUTO_EN)
1	Force free-run mode

**FREE\_RUN\_PAT\_SEL[2:0], Address 0x14[2:0]**

This function selects what data is output in free-run mode.

Table 33. FREE\_FUN\_PAT\_SEL Function

FREE_RUN_PAT_SEL	Description
000 (default)	Single color set by DEF_C and DEF_Y controls; see Color Controls section
001	100% color bars
101	Boundary box



**CLAMP OPERATION**

The input video is ac-coupled into the ADV7182. This has the advantage of protecting the ADV7182 from short-to-battery events. However, the dc value of the input video needs to be restored. This process is referred to as clamping the video. This section explains the general process of clamping on the ADV7182 in both single-ended and differential modes. This section also shows the different ways in which a user can configure clamp operation behavior.

**Single-Ended CVBS Clamp Operation**

The ADV7182 uses a combination of current sources and a digital processing block for clamping, as shown in Figure 15. The analog processing channel shown is replicated three times inside the IC. Whereas only a single channel is needed for a single-ended CVBS signal, two independent channels are needed for Y/C (SVHS) type signals, and three independent channels are needed to allow component signals (YPrPb) to be processed.

The clamping can be divided into two sections:

- Clamping before the ADC (analog domain): current sources and voltage sources.
- Clamping after the ADC (digital domain): digital processing block.

The primary task of the analog clamping circuits is to ensure that the video signal stays within the valid 1.0 V ADC input window so that the analog-to-digital conversion can take place. The current sources in Figure 15 correct the dc level of the ac-coupled input video signal before it is fed into the ADC. The digitized data from the ADC is then fed into the video processor. The digital fine clamp block within the video processor corrects for any remaining variation in the dc level. The video processor also sends clamp control signals to the current sources. This feedback loop fine tunes the current clamp operation and compensates for any noise on the inputted video signal. This maintains the dc level of the video signal during normal operation.

**Differential CVBS Clamping Operation**

The differential clamping operation works in a similar manner to the single-ended clamping operation (see Single-Ended CVBS Clamp Operation section). In differential mode, a coarse clamp pulls the positive and negative video input to a common-mode voltage  $V_{CML}$  (see Figure 16). The feedback loop between the current clamps and the video processor fine tune this coarse dc offset and make the clamping robust to noise on the video input.

Note that the current clamps are controlled within a feedback loop between the AFE and the video processor, and the coarse clamps are not.

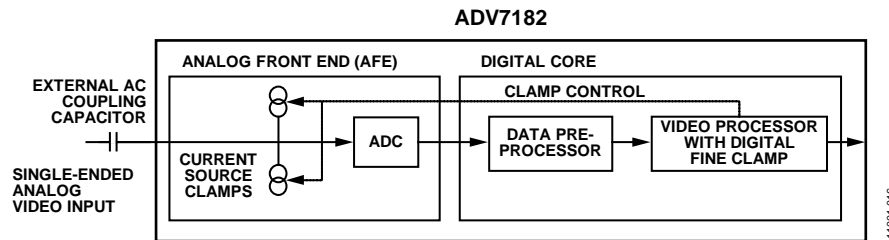


Figure 15. Single-Ended Clamping Overview

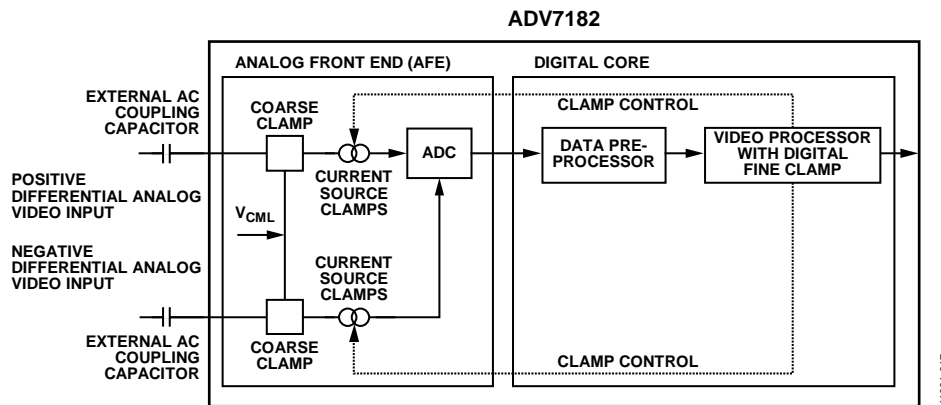


Figure 16. Differential Clamping Overview

### Clamp Operation Controls

The following sections describe the I<sup>2</sup>C signals that can be used to influence the behavior of the clamping block.

#### CCLEN, Current Clamp Enable, Address 0x14[4]

The current clamp enable bit allows the user to switch off all the current sources in the AFE simultaneously. This may be useful if the incoming analog video signal is clamped externally.

When CCLEN is 0, the current sources are switched off.

When CCLEN is 1 (default), the current sources are enabled.

#### DCT[1:0], Digital Clamp Timing, Address 0x15[6:5]

The clamp timing register determines the time constant of the digital fine clamp circuitry. Note that the digital fine clamp reacts quickly because it immediately corrects any residual dc level error for the active line. The time constant from the digital fine clamp must be much quicker than the one from the analog blocks.

By default, the time constant of the digital fine clamp is adjusted dynamically to suit the currently connected input signal.

**Table 34. DCT Function**

DCT[1:0]	Description
00 (default)	Slow (TC = 1 sec)
01	Medium (TC = 0.5 sec)
10	Fast (TC = 0.1 sec)
11	Determined by <a href="#">ADV7182</a> , depending on the input video parameters

#### DCFE, Digital Clamp Freeze Enable, Address 0x15[4]

This register bit allows users to freeze the digital clamp loop at any time (do their own clamping). Users can disable the current sources for analog clamping via the appropriate register bits, wait until the digital clamp loop settles, and then freeze it via the DCFE bit.

When DCFE is set to 0 (default), the digital clamp is operational.

When DCFE is 1, the digital clamp loop is frozen.

### LUMA FILTER

Data from the digital fine clamp block is processed by the three sets of filters that follow. The data format at this point is CVBS for CVBS input or luma only for Y/C and YPrPb input formats.

- Luma antialias filter (YAA). The [ADV7182](#) receives video at a rate of 28.6363 MHz. (In the case of 4× oversampled video, the ADC samples at 57.27 MHz, and the first decimation is performed inside the DPP filters. Therefore, the data rate into the [ADV7182](#) is always 28.6363 MHz.) The ITU-R BT.601 recommends a sampling frequency of 13.5 MHz. The luma antialias filter decimates the oversampled video using a high quality linear phase, low-pass filter that preserves the luma signal while, at the same time, attenuating out-of-band components. The luma antialias filter (YAA) has a fixed response.
- Luma shaping filters (YSH). The shaping filter block is a programmable low-pass filter with a wide variety of responses. It can be used to reduce selectively the luma video signal bandwidth (needed prior to scaling, for example). For some video sources that contain high frequency noise, reducing the bandwidth of the luma signal improves visual picture quality. If the video is low-pass filtered, a follow-on video compression stage can work more efficiently. The [ADV7182](#) has two responses for the shaping filter: one that is used for good quality composite, component, and SVHS type sources; and a second for nonstandard CVBS signals. The YSH filter responses also include a set of notches for PAL and NTSC. However, using the comb filters for Y/C separation is recommended.
- Digital resampling filter. This block allows dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system with no requirement for user intervention.

Figure 18 through Figure 21 show the overall response of all filters together. Unless otherwise noted, the filters are set into a typical wideband mode.

### Y Shaping Filter

For input signals in CVBS format, the luma shaping filters play an essential role in removing the chroma component from a composite signal. Y/C separation must aim for best possible crosstalk reduction while still retaining as much bandwidth (especially on the luma component) as possible. High quality Y/C separation can be achieved by using the internal comb filters of the ADV7182. Comb filtering, however, relies on the frequency relationship of the luma component (multiples of the video line rate) and the color subcarrier ( $f_{sc}$ ). For good quality CVBS signals, this relationship is known; the comb filter algorithms can be used to separate luma and chroma with high accuracy.

In the case of nonstandard video signals, the frequency relationship may be disturbed, and the comb filters may not be able to remove all crosstalk artifacts in the best fashion without the assistance of the shaping filter block.

An automatic mode is provided that allows the ADV7182 to evaluate the quality of the incoming video signal and select the filter responses in accordance with the signal quality and video standard. YFSM, WYSFMOVR, and WYSFM allow the user to manually override the automatic decisions in part or in full.

The luma shaping filter has the following control bits.

- YFSM[4:0] allows the user to manually select a shaping filter mode (applied to all video signals) or to enable an automatic selection (depending on video quality and video standard).
- WYSFMOVR allows the user to manually override the WYSFM decision.
- WYSFM[4:0] allows the user to select a different shaping filter mode for good quality composite (CVBS), component (YPrPb), and SVHS (Y/C) input signals.

In automatic mode, the system preserves the maximum possible bandwidth for good CVBS sources (because they can be successfully combed) as well as for luma components of YPrPb and Y/C sources (because they need not be combed). For poor quality signals, the system selects from a set of proprietary shaping filter responses that complements comb filter operation to reduce visual artifacts.

The decisions of the control logic are shown in Figure 17.

#### YFSM[4:0], Y Shaping Filter Mode, Address 0x17[4:0]

The Y shaping filter mode bits allow the user to select from a wide range of low-pass and notch filters. When switched in automatic mode, the filter selection is based on other register selections, such as detected video standard, as well as properties extracted from the incoming video itself, such as quality and time base stability. The automatic selection always selects the widest possible bandwidth for the video input encountered. (See Table 35.)

The Y-shaping filter mode operates as follows:

- If the YFSM settings specify a filter (that is, YFSM is set to values other than 00000 or 00001), the chosen filter is applied to all video, regardless of its quality.
- In automatic selection mode, the notch filters are only used for bad quality video signals. For all other video signals, wideband filters are used.

#### WYSFMOVR, Wideband Y Shaping Filter Override, Address 0x18[7]

Setting the WYSFMOVR bit enables the use of the WYSFM[4:0] settings for good quality video signals. For more information on luma shaping filters, see the Y Shaping Filter section and the flowchart shown in Figure 17.

When WYSFMOVR is set to 0, the shaping filter for good quality video signals is selected automatically.

Setting WYSFMOVR is set to 1 (default), it enables manual override via WYSFM[4:0].

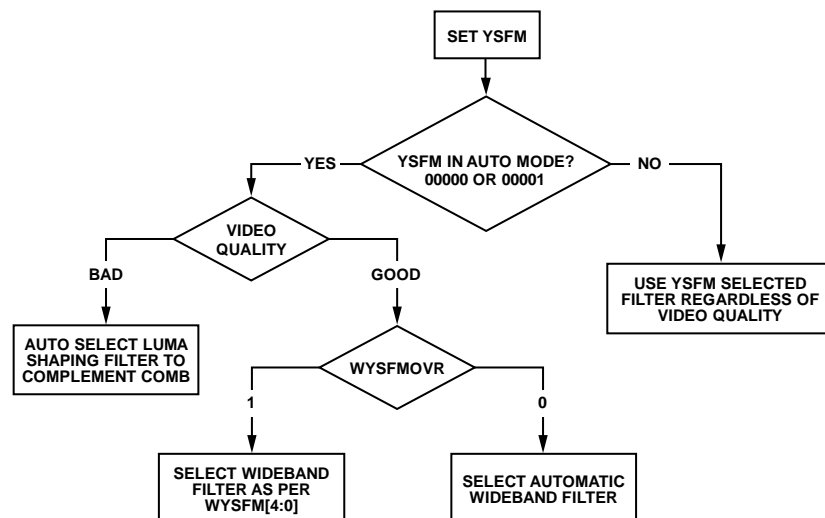


Figure 17. YFSM and WYSFM Control Flowchart

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Table 35. YSFM Function

YSFM[4:0]	Description
00000	Automatic selection including a wide notch response (PAL/NTSC/SECAM)
00001 (default)	Automatic selection including a narrow notch response (PAL/NTSC/SECAM)
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011	SVHS 18 (CCIR 601)
10100	PAL NN1
10101	PAL NN2
10110	PAL NN3
10111	PAL WN1
11000	PAL WN2
11001	NTSC NN1
11010	NTSC NN2
11011	NTSC NN3
11100	NTSC WN1
11101	NTSC WN2
11110	NTSC WN3
11111	Reserved

**WYSFM[4:0], Wideband Y Shaping Filter Mode, Address 0x18[4:0]**

The WYSFM[4:0] bits allow the user to manually select a shaping filter for good quality video signals, for example, CVBS with stable time base, luma component of YPrPb, and luma component of Y/C. The WYSFM bits are active only if the WYSFMOVR bit is set to 1. See the general discussion of the shaping filter settings in the Y Shaping Filter section.

Table 36. WYSFM Function

WYSFM[4:0]	Description
00000	Reserved, do not use
00001	Reserved, do not use
00010	SVHS 1
00011	SVHS 2
00100	SVHS 3
00101	SVHS 4
00110	SVHS 5
00111	SVHS 6
01000	SVHS 7
01001	SVHS 8
01010	SVHS 9
01011	SVHS 10
01100	SVHS 11
01101	SVHS 12
01110	SVHS 13
01111	SVHS 14
10000	SVHS 15
10001	SVHS 16
10010	SVHS 17
10011 (default)	SVHS 18 (CCIR 601)
10100 to 11111	Reserved, do not use

The filter plots in Figure 18 show the SVHS 1 (narrowest) to SVHS 18 (widest) shaping filter settings. Figure 20 shows the PAL notch filter responses. The NTSC notch filter responses are shown in Figure 21.

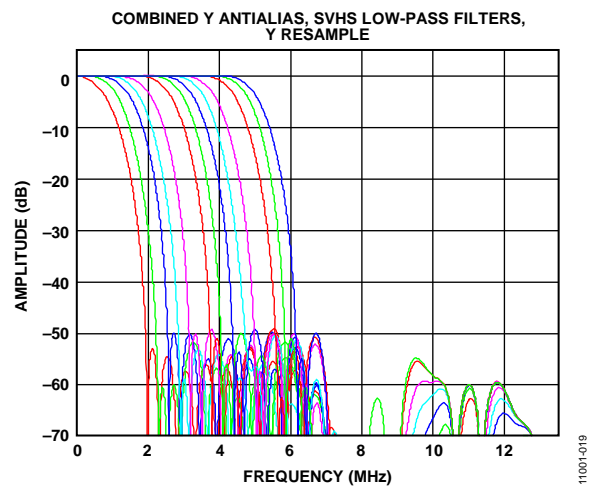


Figure 18. Y SVHS Combined Responses

**CHROMA FILTER**

Data from the digital fine clamp block is processed by the three sets of filters that follow. The data format at this point is CVBS for CVBS inputs, chroma only for Y/C, or U/V interleaved for YPrPb input formats.

- Chroma antialias filter (CAA). The ADV7182 oversamples the CVBS by a factor of 4 and the chroma/YPrPb by a factor of 2. A decimating filter (CAA) is used to preserve the active video band and to remove any out-of-band components. The CAA filter has a fixed response.
- Chroma shaping filters (CSH). The shaping filter block (CSH) can be programmed to perform a variety of low-pass responses. It can be used to selectively reduce the bandwidth of the chroma signal for scaling or compression.
- Digital resampling filter. This block allows dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system without user intervention.

Figure 22 shows the overall response of all filters together.

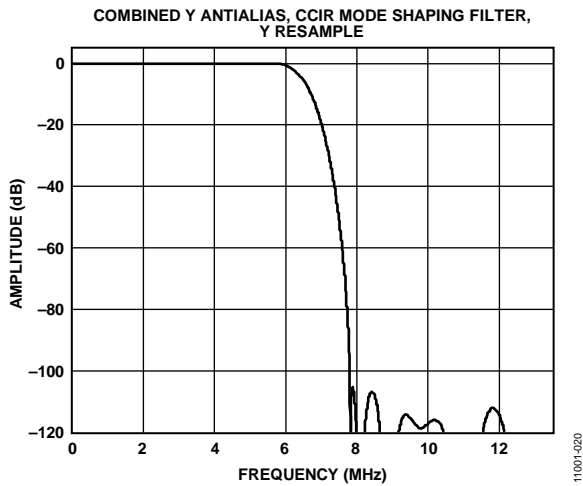


Figure 19. Combined Y Antialias, CCIR Mode Shaping Filter

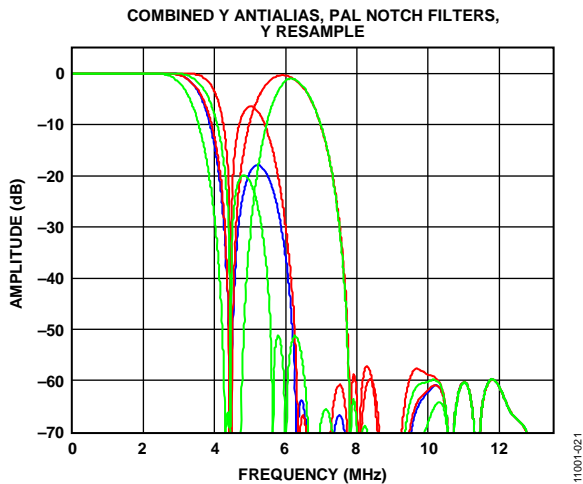


Figure 20. Combined Y Antialias, PAL Notch Filters

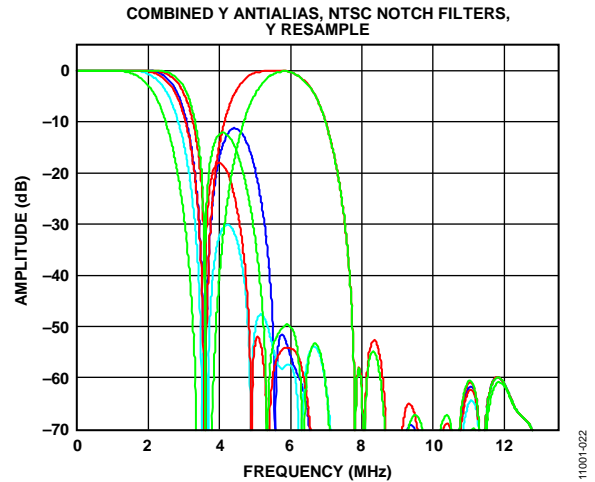


Figure 21. Combined Y Antialias Filter, NTSC Notch Filters

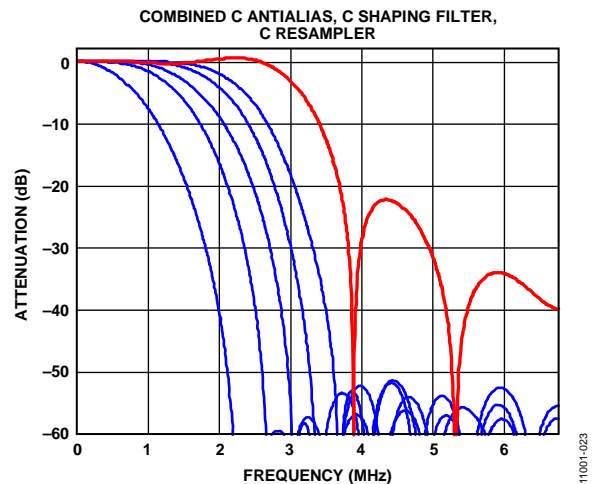


Figure 22. Chroma Shaping Filter Responses

**CSFM[2:0], C Shaping Filter Mode, Address 0x17[7:5]**

The C shaping filter mode bits allow the user to select from a range of low-pass filters for the chrominance signal. When switched in automatic mode, the widest filter is selected based on the video standard/format and user choice (see the 000 and 001 settings in Table 37).

**Table 37. CSFM Function**

CSFM[2:0]	Description
000 (default)	Autoselection 1.5 MHz bandwidth
001	Autoselection 2.17 MHz bandwidth
010	SH1
011	SH2
100	SH3
101	SH4
110	SH5
111	Wideband mode

Figure 22 shows the responses of SH1 (narrowest) to SH5 (widest) in addition to the wideband mode (shown in red).

**GAIN OPERATION**

The gain control within the ADV7182 is done on a purely digital basis. The input ADC supports a 10-bit range mapped into a 1.0 V analog voltage range. Gain correction takes place after the digitization in the form of a digital multiplier.

Advantages of this architecture over the commonly used programmable gain amplifier (PGA) before the ADC include the fact that the gain is now completely independent of supply, temperature, and process variations.

As shown in Figure 25, the ADV7182 can decode a video signal as long as it fits into the ADC window. The components for this are the amplitude of the input signal and the dc level it resides on. The dc level is set by the clamping circuitry (see the Clamp Operation section).

If the amplitude of the analog video signal is too high, clipping may occur, resulting in visual artifacts. The analog input range of the ADC, together with the clamp level, determines the maximum supported amplitude of the video signal.

Figure 23 and Figure 24 show the typical voltage divider networks required to keep the input video signal within the allowed range of the ADC, 0 V to 1 V. Place the circuit in Figure 23 before all the single-ended analog inputs to the ADV7182, and place the circuit in Figure 24 before all the differential inputs to the ADV7182.

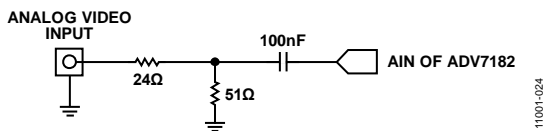


Figure 23. Single-Ended Input Voltage Divider Network

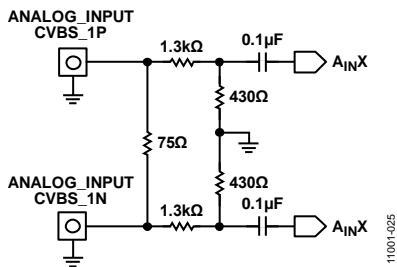


Figure 24. Differential Input Voltage Divider Network

The minimum supported amplitude of the input video is determined by the ability of the ADV7182 to retrieve horizontal and vertical timing and to lock to the color burst, if present.

There are separate gain control units for luma and chroma data. Both can operate independently of each other. The chroma unit, however, can also take its gain value from the luma path.

The possible AGC modes are shown in Table 38.

**Table 38. AGC Modes**

Input Video Type	Luma Gain	Chroma Gain
Any	Manual gain luma	Manual gain chroma
CVBS	Dependent on horizontal sync depth Peak white	Dependent on color-burst amplitude taken from luma path Dependent on color-burst amplitude taken from luma path
Y/C	Dependent on horizontal sync depth Peak white	Dependent on color-burst amplitude taken from luma path Dependent on color-burst amplitude
YPrPb	Dependent on horizontal sync depth	Taken from luma path

It is possible to freeze the automatic gain control loops. This causes the loops to stop updating and the AGC determined gain at the time of the freeze to stay active until the loop is either unfrozen or the gain mode of operation is changed.

The currently active gain from any of the modes can be read back. Refer to the description of the dual-function manual gain registers, LG[11:0] luma gain and CG[11:0] chroma gain, in the Luma Gain and Chroma Gain sections.

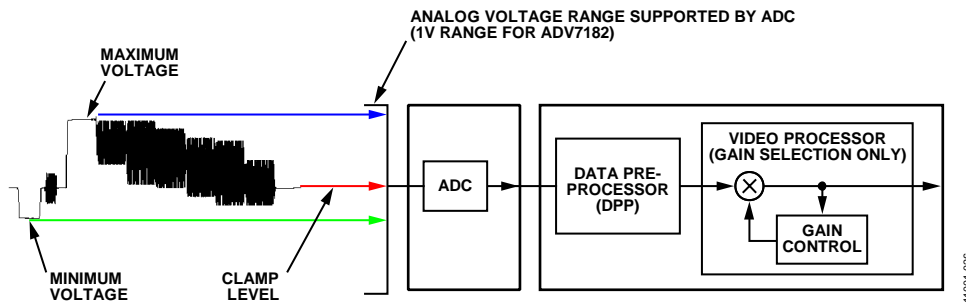


Figure 25. Gain Control Overview

**Luma Gain**

**LAGC[2:0], Luma Automatic Gain Control, Address 0x2C[6:4]**

The luma automatic gain control mode bits select the operating mode for the gain control in the luma path.

There are internal parameters (Analog Devices proprietary algorithms) to customize the peak white gain control. Contact local Analog Devices field applications engineers or a local Analog Devices distributor for more information.

**Table 39. LAGC Function**

LAGC[2:0]	Description
000	Manual fixed gain (use LMG[11:0])
001	AGC (blank level to sync tip), peak white algorithm off
010 (default)	AGC (blank level to sync tip), peak white algorithm on
011	Reserved
100	Reserved
101	Reserved
110	Reserved
111	Freeze gain

**LAGT[1:0], Luma Automatic Gain Timing, Address 0x2F[7:6]**

The luma automatic gain timing register allows the user to influence the tracking speed of the luminance automatic gain control. This register has an effect only if the LAGC[2:0] register is set to 001 or 010 (automatic gain control modes).

If peak white AGC is enabled and active (see the Status 1[7:0], Address 0x10[7:0] section), the actual gain update speed is dictated by the peak white AGC loop and, as a result, the LAGT settings have no effect. As soon as the part leaves peak white AGC, LAGT becomes relevant again.

The update speed for the peak white algorithm can be customized by the use of internal parameters. Contact Analog Devices local field engineers for more information.

**Table 40. LAGT Function**

LAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Fast (TC = 0.2 sec)
11 (default)	Adaptive

**LG[11:0], Luma Gain, Address 0x2F[3:0], Address 0x30[7:0]**

**LMG[11:0], Luma Manual Gain, Address 0x2F[3:0], Address 0x30[7:0]**

Luma gain[11:0] is a dual-function register. If all these bits are written to, a desired manual luma gain can be programmed. This gain becomes active if the LAGC[2:0] mode is switched to manual fixed gain. Equation 1 shows how to calculate a desired gain.

If read back, this register returns the current gain value.

Depending on the setting in the LAGC[2:0] bits, the value is one of the following:

- Luma manual gain value (LAGC[2:0] set to luma manual gain mode)
- Luma automatic gain value (LAGC[2:0] set to either of the automatic modes)

**Table 41. LG/LMG Function**

LG[11:0]/LMG[11:0]	Read/Write	Description
LMG[11:0] = x	Write	Manual gain for luma path
LG[11:0] = x	Read	Actual used gain

$$Luma\ Gain \cong \frac{LMG[11:0]}{Luma\ Calibration\ Factor} \quad (1)$$

where  $LMG[11:0]$  is a decimal value between 1024 and 4095.

**Calculation of the Luma Calibration Factor**

1. Using a video source, set the content to a gray field and apply as a standard CVBS signal to the CVBS input of the board.
2. Using an oscilloscope, measure the signal at the CVBS input to ensure that its sync depth, color burst, and luma are at the standard levels.
3. Connect the output parallel pixel bus of the [ADV7182](#) to a backend system that has unity gain and monitor the output voltage.
4. Measure the luma level correctly from the black level. Turn off the luma AGC and manually change the value of the luma manual gain control register, LMG[11:0], until the output luma level matches the input measured in Step 2.

This value, in decimal, is the luma calibration factor.

**BETACAM, Enable Betacam Levels, Address 0x01[5]**

If YPrPb data is routed through the [ADV7182](#), the automatic gain control modes can target different video input levels, as outlined in Table 45. The BETACAM bit is valid only if the input mode is YPrPb (component). The BETACAM bit sets the target value for AGC operation.

A review of the following sections is useful:

- The MAN\_MUX\_EN, Manual Input Muxing Enable, Address 0xC4[7] section for how component video (YPrPb) can be routed through the [ADV7182](#).
- The Video Standard Selection section to select the various standards, for example, with and without pedestal.

The AGC algorithms adjust the levels based on the setting of the BETACAM bit (see Table 44).

**PW\_UPD, Peak White Update, Address 0x2B[0]**

The peak white and average video algorithms determine the gain based on measurements taken from the active video. The PW\_UPD bit determines the rate of gain change. LAGC[2:0] must be set to the appropriate mode to enable the peak white or average video mode in the first place. For more information, see the LAGC[2:0], Luma Automatic Gain Control, Address 0x2C[6:4] section.

Setting PW\_UPD to 0 updates the gain once per video line.

Setting PW\_UPD to 1 (default) updates the gain once per field.

**Table 44. BETACAM Function**

BETACAM	Description
0 (default)	Assuming YPrPb is selected as input format: Selecting PAL with pedestal selects MII. Selecting PAL without pedestal selects SMPTE. Selecting NTSC with pedestal selects MII. Selecting NTSC without pedestal selects SMPTE.
1	Assuming YPrPb is selected as input format: Selecting PAL with pedestal selects BETACAM. Selecting PAL without pedestal selects BETACAM variant. Selecting NTSC with pedestal selects BETACAM. Selecting NTSC without pedestal selects BETACAM variant.

**Table 45. BETACAM Levels**

Name	BETACAM (mV)	BETACAM Variant (mV)	SMPTE (mV)	III (mV)
Y	0 to +714 (including 7.5% pedestal)	0 to +714	0 to +700	0 to +700 (including 7.5% pedestal)
Pb and Pr	-467 to +467	-505 to +505	-350 to +350	-324 to +324
Sync Depth	+286	+286	+300	+300

**Chroma Gain**

**CAGC[1:0], Chroma Automatic Gain Control, Address 0x2C[1:0]**

The two bits of the color automatic gain control mode select the basic mode of operation for the automatic gain control in the chroma path.

**Table 42. CAGC Function**

CAGC[1:0]	Description
00	Manual fixed gain (use CMG[11:0])
01	Use Luma gain for chroma
10 (default)	Automatic gain (based on color burst)
11	Freeze chroma gain

**CAGT[1:0], Chroma Automatic Gain Timing, Address 0x2D[7:6]**

The chroma automatic gain timing register allows the user to influence the tracking speed of the chroma automatic gain control. This register has an effect only if the CAGC[1:0] bits are set to 10 (automatic gain).

**Table 43. CAGT Function**

CAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Reserved
11 (default)	Adaptive



**CG[11:0], Chroma Gain, Address 0x2D[3:0],  
Address 0x2E[7:0]; CMG[11:0], Chroma Manual Gain,  
Address 0x2D[3:0], Address 0x2E[7:0]**

Chroma gain[11:0] is a dual-function register. If written to, a desired manual chroma gain can be programmed. This gain becomes active if the CAGC[1:0] function is switched to manual fixed gain. See Equation 2 for calculating a desired gain.

If read back, this register returns the current gain value. Depending on the setting in the CAGC[1:0] bits, this is either:

- The chroma manual gain value (CAGC[1:0] set to chroma manual gain mode).
- The chroma automatic gain value (CAGC[1:0] set to either of the automatic modes).

**Table 46. CG/CMG Function**

CG[11:0]/CMG[11:0]	Read/Write	Description
CMG[11:0]	Write	Manual gain for chroma path
CG[11:0]	Read	Currently active gain

$$Chroma\_Gain \cong \frac{CMG[11:0]_{decimal}}{ChromaCalibrationFactor} \quad (2)$$

where *ChromaCalibrationFactor* is a decimal value between 0 and 4095.

**Calculation of Chroma Calibration Factor**

Take the following steps to calculate the chroma calibration factor:

1. Apply a CVBS signal with the color bars/SMPTE bars test pattern content directly to the measurement equipment.
2. Ensure correct termination of 75 Ω on the measurement equipment. Measure chroma output levels.
3. Reconnect the source to the CVBS input of the [ADV7182](#) system that has a back end gain of 1. Repeat the measurement of chroma levels.
4. Turn off the chroma AGC and manually change the chroma gain control register, CMG[11:0], until the chroma level matches that measured directly from the source.

This value, in decimal, is the chroma calibration factor.

**CKE, Color Kill Enable, Address 0x2B[6]**

The color kill enable bit allows the optional color kill function to be switched on or off.

For QAM-based video standards (PAL and NTSC), as well as FM-based systems (SECAM), the threshold for the color kill decision is selectable via the CKILLTHR[2:0] bits.

If color kill is enabled and the color carrier of the incoming video signal is less than the threshold for 128 consecutive video lines, color processing is switched off (black and white output). To switch the color processing back on, another 128 consecutive lines with a color burst greater than the threshold are required.

The color kill option works only for input signals with a modulated chroma part. For component input (YPrPb), there is no color kill.

Set CKE to 0 to disable color kill.

Set CKE to 1 (default) to enable color kill.

**CKILLTHR[2:0], Color Kill Threshold, Address 0x3D[6:4]**

The CKILLTHR[2:0] bits allow the user to select a threshold for the color kill function. The threshold applies only to QAM-based (NTSC and PAL) or FM-modulated (SECAM) video standards.

To enable the color kill function, the CKE bit must be set. For the 000, 001, 010, and 011 settings, chroma demodulation inside the [ADV7182](#) may not work satisfactorily for poor input video signals.

**Table 47. CKILLTHR Function**

CKILLTHR[2:0]	Description	
	NTSC, PAL	SECAM
000	Kill at <0.5%	No color kill
001	Kill at <1.5%	Kill at <5%
010 (default)	Kill at <2.5%	Kill at <7%
011	Kill at <4%	Kill at <8%
100	Kill at <8.5%	Kill at <9.5%
101	Kill at <16%	Kill at <15%
110	Kill at <32%	Kill at <32%
111	Reserved for Analog Devices internal use only; do not select	

**CHROMA TRANSIENT IMPROVEMENT (CTI)**

The signal bandwidth allocated for chroma is typically much smaller than that for luminance. In the past, this was a valid way to fit a color video signal into a given overall bandwidth because the human eye is less sensitive to chrominance than to luminance.

The uneven bandwidth, however, may lead to visual artifacts in sharp color transitions. At the border of two bars of color, both components (luma and chroma) change at the same time (see Figure 26). Due to the higher bandwidth, the signal transition of the luma component is usually much sharper than that of the chroma component. The color edge is not sharp, and in the worst case, it can be blurred over several pixels.

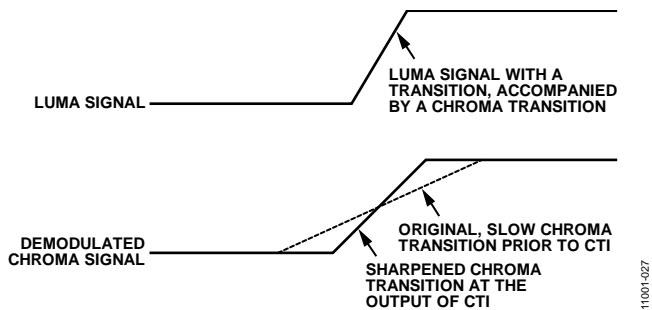


Figure 26. CTI Luma/Chroma Transition

The chroma transient improvement block examines the input video data. It detects transitions of chroma and can be programmed to create steeper chroma edges in an attempt to artificially restore lost color bandwidth. The CTI block, however, operates only on edges above a certain threshold to ensure that noise is not emphasized. Care was taken to ensure that edge ringing and undesirable saturation or hue distortion are avoided.

Chroma transient improvements are needed primarily for signals that have severe chroma bandwidth limitations. For those types of signals, it is strongly recommended to enable the CTI block via CTI\_EN.

**CTI\_EN, Chroma Transient Improvement (CTI) Enable, Address 0x4D[0]**

Set CTI\_EN to 0 to disable the CTI block.

Set CTI\_EN to 1 (default) to enable the CTI block.

**CTI\_AB\_EN, Chroma Transient Improvement Alpha Blend Enable, Address 0x4D[1]**

The CTI\_AB\_EN bit enables an alpha blend function within the CTI block. If set to 1, the alpha blender mixes the transient improved chroma with the original signal. The sharpness of the alpha blending can be configured via the CTI\_AB[1:0] bits.

For the alpha blender to be active, the CTI block must be enabled via the CTI\_EN bit.

Set CTI\_AB\_EN to 0 to disable the CTI alpha blender.

Set CTI\_AB\_EN to 1 (default) to enable the CTI alpha-blend mixing function.

**CTI\_AB[1:0], Chroma Transient Improvement Alpha Blend, Address 0x4D[3:2]**

The CTI\_AB[1:0] controls the behavior of alpha-blend circuitry that mixes the sharpened chroma signal with the original one. It thereby controls the visual impact of CTI on the output data.

For CTI\_AB[1:0] to become active, the CTI block must be enabled via the CTI\_EN bit, and the alpha blender must be switched on via CTI\_AB\_EN.

Sharp blending maximizes the effect of CTI on the picture; however, it may also increase the visual impact of small amplitude, high frequency chroma noise.

Table 48. CTI\_AB Function

CTI_AB[1:0]	Description
00	Sharpest mixing between sharpened and original chroma signal
01	Sharp mixing
10	Smooth mixing
11 (default)	Smoothest mixing between sharpened and original chroma signal

**CTI\_C\_TH[7:0], CTI Chroma Threshold, Address 0x4E[7:0]**

The CTI\_C\_TH[7:0] value is an unsigned, 8-bit number specifying how big the amplitude step in a chroma transition must be if it is going to be steepened by the CTI block. Programming a small value into this register causes even smaller edges to be steepened by the CTI block. Making CTI\_C\_TH[7:0] a large value causes the block to improve large transitions only.

The default value for CTI\_C\_TH[7:0] is 0x08.

**DIGITAL NOISE REDUCTION (DNR) AND LUMA PEAKING FILTER**

Digital noise reduction is based on the assumption that high frequency signals with low amplitude are probably noise and that their removal, therefore, improves picture quality. The two DNR blocks in the ADV7182 are the DNR1 block before the luma peaking filter and the DNR2 block after the luma peaking filter, as shown in Figure 27.

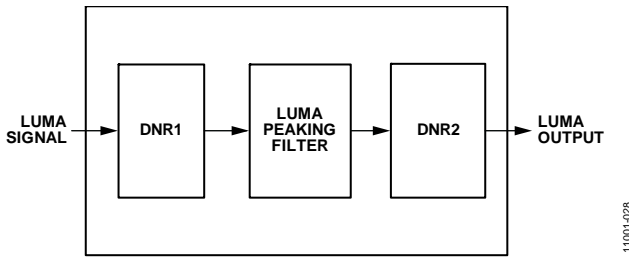


Figure 27. DNR and Peaking Block Diagram

**DNR\_EN, Digital Noise Reduction Enable, Address 0x4D[5]**

The DNR\_EN bit enables the DNR block or bypasses it.

Table 49. DNR\_EN Function

Setting	Description
0	Bypasses the DNR block (disable)
1 (default)	Enables the DNR block

**DNR\_TH[7:0], DNR Noise Threshold 1, Address 0x50[7:0]**

The DNR1 block is positioned before the luma peaking block. The DNR\_TH[7:0] value is an unsigned, 8-bit number used to determine the maximum edge that is interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR\_TH[7:0] causes the DNR block to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and to be removed.

Table 50. DNR\_TH[7:0] Function

Setting	Description
0x08 (default)	Threshold for maximum luma edges to be interpreted as noise

**PEAKING\_GAIN[7:0], Luma Peaking Gain, Address 0xFB[7:0]**

This filter can be manually enabled. The user can select to boost or to attenuate the midregion of the Y spectrum around 3 MHz. The peaking filter can visually improve the picture by showing more definition on the picture details that contain frequency components around 3 MHz. The default value on this register passes through the luma data unaltered. A lower value attenuates the signal, and a higher value gains the luma signal. A plot of the responses of the filter is shown in Figure 28.

Table 51. PEAKING\_GAIN[7:0] Function

Setting	Description
0x40 (default)	0 dB response

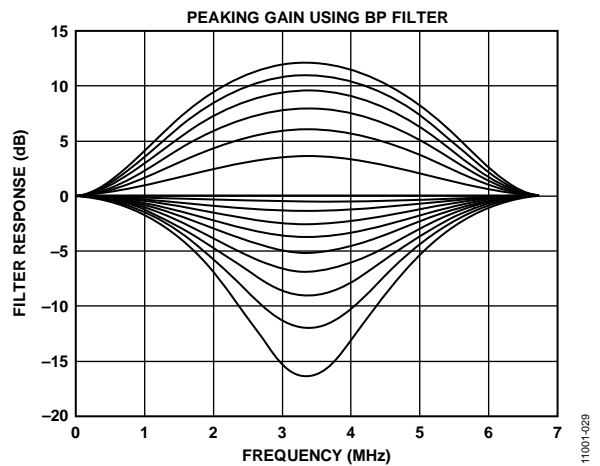


Figure 28. Peaking Filter Responses

**DNR\_TH2[7:0], DNR Noise Threshold 2, Address 0xFC[7:0]**

The DNR2 block is positioned after the luma peaking block and, therefore, affects the gained luma signal. It operates in the same way as the DNR1 block; however, there is an independent threshold control, DNR\_TH2[7:0], for this block. This value is an unsigned, 8-bit number used to determine the maximum edge that is interpreted as noise and, therefore, blanked from the luma data. Programming a large value into DNR\_TH2[7:0] causes the DNR block to interpret even large transients as noise and remove them. As a result, the effect on the video data is more visible. Programming a small value causes only small transients to be seen as noise and to be removed.

Table 52. DNR\_TH2[7:0] Function

Setting	Description
0x04 (default)	Threshold for maximum luma edges to be interpreted as noise

**COMB FILTERS**

The comb filters of the ADV7182 can automatically handle video of all types, standards, and levels of quality. The NTSC and PAL configuration registers allow the user to customize the comb filter operation depending on which video standard is detected (by autodetection) or selected (by manual programming). In addition to the bits listed in this section, there are some other internal controls (based on Analog Devices proprietary algorithms); contact local Analog Devices field engineers for more information.

**NTSC Comb Filter Settings**

These settings are used for NTSC M/NTSC J CVBS inputs.

**NSFSEL[1:0], Split Filter Selection, NTSC, Address 0x19[3:2]**

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A narrow split filter selection results in better performance on diagonal lines but more dot crawl in the final output image. The opposite is true for selecting a wide bandwidth split filter.

**Table 53. NSFSEL Function**

NSFSEL[1:0]	Description
00 (default)	Narrow
01	Medium
10	Medium
11	Wide

**CTAPSN[1:0], Chroma Comb Taps, NTSC, Address 0x38[7:6]****Table 54. CTAPSN Function**

CTAPSN[1:0]	Description
00	Do not use
01	NTSC chroma comb adapts three lines to two lines
10 (default)	NTSC chroma comb adapts five lines to three lines
11	NTSC chroma comb adapts five lines to four lines

**CCMN[2:0], Chroma Comb Mode, NTSC, Address 0x38[5:3]****Table 55. CCMN Function**

CCMN[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Three-line adaptive chroma comb for CTAPSN = 01 Four-line adaptive chroma comb for CTAPSN = 10 Five-line adaptive chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01  Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01 Fixed four-line chroma comb for CTAPSN = 10 Fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01  Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11

## YCMN[2:0], Luma Comb Mode, NTSC, Address 0x38[2:0]

Table 56. YCMN Function

YCMN[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-lines (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed luma comb two-line (two taps)
110	Fixed luma comb (all lines of line memory)	Fixed luma comb three-line (three taps)
111	Fixed luma comb (bottom lines of line memory)	Fixed luma comb two-line (two taps)

**PAL Comb Filter Settings**

These settings are used for PAL B/PAL G/PAL H/PAL I/PAL D, PAL M, PAL Combinational N, PAL 60, and NTSC 4.43 CVBS inputs.

**PSFSEL[1:0], Split Filter Selection, PAL, Address 0x19[1:0]**

The PSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A wide split filter selection eliminates dot crawl but shows imperfections on diagonal lines. The opposite is true for selecting a narrow bandwidth split filter.

Table 57. PSFSEL Function

PSFSEL[1:0]	Description
00	Narrow
01 (default)	Medium
10	Wide
11	Widest

## CTAPSP[1:0], Chroma Comb Taps, PAL, Address 0x39[7:6]

Table 58. CTAPSP Function

CTAPSP[1:0]	Description
00	Do not use
01	PAL chroma comb adapts five lines (three taps) to three lines (two taps); cancels cross luma only
10	PAL chroma comb adapts five lines (five taps) to three lines (three taps); cancels cross luma and hue error less well
11 (default)	PAL chroma comb adapts five lines (five taps) to four lines (four taps); cancels cross luma and hue error well

## CCMP[2:0], Chroma Comb Mode, PAL, Address 0x39[5:3]

Table 59. CCMP Function

CCMP[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive three-line chroma comb for CTAPSN = 01 Adaptive four-line chroma comb for CTAPSN = 10 Adaptive five-line chroma comb for CTAPSN = 11
100	Disable chroma comb	
101	Fixed chroma comb (top lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01  Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11
110	Fixed chroma comb (all lines of line memory)	Fixed three-line chroma comb for CTAPSN = 01 Fixed four-line chroma comb for CTAPSN = 10 Fixed five-line chroma comb for CTAPSN = 11
111	Fixed chroma comb (bottom lines of line memory)	Fixed two-line chroma comb for CTAPSN = 01  Fixed three-line chroma comb for CTAPSN = 10 Fixed four-line chroma comb for CTAPSN = 11

## YCMP[2:0], Luma Comb Mode, PAL, Address 0x39[2:0]

Table 60. YCMP Function

YCMP[2:0]	Description	Configuration
000 (default)	Adaptive comb mode	Adaptive five lines (three taps) luma comb
100	Disable luma comb	Use low-pass/notch filter; see the Y Shaping Filter section
101	Fixed luma comb (top lines of line memory)	Fixed three lines (two taps) luma comb
110	Fixed luma comb (all lines of line memory)	Fixed five lines (three taps) luma comb
111	Fixed luma comb (bottom lines of line memory)	Fixed three lines (two taps) luma comb

**IF FILTER COMPENSATION**

**IFFILTSEL[2:0], IF Filter Select, Address 0xF8[2:0]**

The IFFILTSEL[2:0] register allows the user to compensate for SAW filter characteristics on a composite input, as would be observed on tuner outputs. Figure 29 and Figure 30 show IF filter compensation for NTSC and PAL, respectively.

The options for this feature are as follows:

- Bypass mode
- NTSC, consisting of three filter characteristics
- PAL, consisting of three filter characteristics

See Table 94 for programming details.

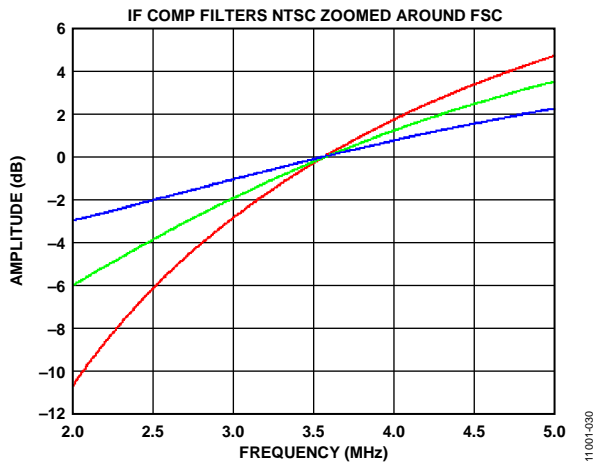


Figure 29. NTSC IF Filter Compensation

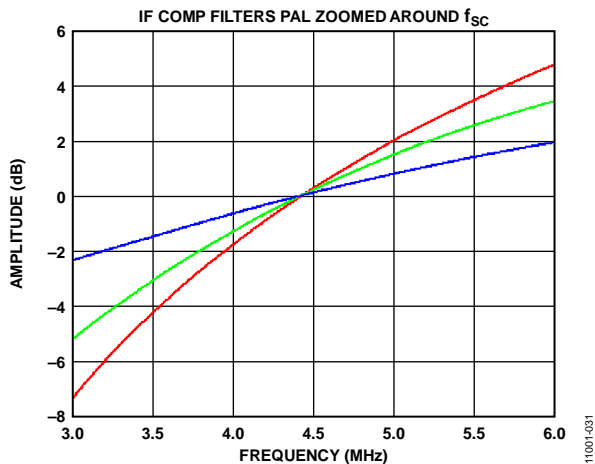


Figure 30. PAL IF Filter Compensation

**ADAPTIVE CONTRAST ENHANCEMENT (ACE)**

ACE allows for the contrast of an image to be increased, depending on the content of the picture. Normally, this allows bright areas to be made brighter and dark areas to be made darker. However, the ADV7182 ACE feature also allows for the contrast within dark areas to be increased without significantly affecting bright areas. This is particularly useful in automotive applications where it can be important to be able to discern objects in shaded areas.

The ACE feature works by sampling the chroma and luma levels in the inputted image. This information is then histogrammed, and the resulting correction is applied to the entire image. This correction is done in a nonlinear fashion so that more correction can be applied to dark areas if required.

For normal use, the luma and chroma gain controls can be used; however, in automotive applications, where dark areas may need to be further enhanced, also use the gamma gain controls.

The reaction time of the ACE function can be set using the ACE\_RESPONSE\_SPEED[7:4] bits (see Table 95). The corrected image is faded over the original image using alpha blending, giving a gradual change in contrast with scene changes. The ACE\_RESPONSE\_SPEED[7:4] bits determine the duration of the transition from the original to the corrected image. A larger value for these bits results in a faster transition time; however, a smaller value gives more stability to rapid scene changes.

The ACE\_CHROMA\_MAX[7:4] bits are used to set a maximum value that clips the chroma gain regardless of the ACE\_CHROMA\_GAIN[3:0] settings.

The ACE\_GAMMA\_GAIN[3:0] bits are particularly useful in automotive applications because they allow dramatic image enhancement in dark regions by stretching the contrast of pixels at the low (dark) values of the image histogram. The luma and chroma gain controls are normally used; however, the ACE\_GAMMA\_GAIN[3:0] bits should be used when further stretching of the contrast in the dark areas of an image is needed.

**ACE\_ENABLE, User Sub Map 2, Address 0x80[7]**

Enables ACE.

**Table 61. ACE\_ENABLE Function**

ACE_ENABLE	Description
0 (default)	Disable ACE
1	Enable ACE

**ACE\_LUMA\_GAIN[4:0], User Sub Map 2, Address 0x83[4:0]**

A control to set the auto-contrast level for the luma channel when ACE\_ENABLE is 1.

**Table 62. ACE\_LUMA\_GAIN Function**

ACE_LUMA_GAIN[4:0]	Description
00000	Set ACE luma auto-contrast level to minimum value
01101 (default)	Set ACE luma auto-contrast level to default value
11111	Set ACE luma auto-contrast level to maximum value

**ACE\_RESPONSE\_SPEED[3:0], User Sub Map 2, Address 0x85[7:4]**

Sets the reaction time of the ACE function.

**Table 63. ACE\_RESPONSE\_SPEED Function**

ACE_RESPONSE_SPEED[3:0]	Description
0000	Set speed of ACE response to slowest value
1111 (default)	Set speed of ACE response to fastest value

**ACE\_CHROMA\_GAIN[3:0], User Sub Map 2, Address 0x84[3:0]**

This control sets the color-saturation level for the color channels when ACE\_ENABLE is 1.

**Table 64. ACE\_CHROMA\_GAIN Function**

ACE_CHROMA_GAIN[3:0]	Description
0000	Set ACE color auto-saturation level to minimum value
1000 (default)	Set ACE color auto-saturation level to default value
1111	Set ACE color auto-saturation level to maximum value

**ACE\_CHROMA\_MAX[3:0], User Sub Map 2, Address 0x84[7:4]**

This control sets a maximum threshold value that clips the chroma gain regardless of the ACE\_CHROMA\_GAIN[3:0] settings.

**Table 65. ACE\_CHROMA\_MAX Function**

ACE_CHROMA_MAX[3:0]	Description
0000	Set maximum threshold for ACE color auto-saturation level to minimum value
1000 (default)	Set maximum threshold for ACE color auto-saturation level to default value
1111	Set maximum threshold for ACE color auto-saturation level to maximum value

**ACE\_GAMMA\_GAIN[3:0], User Sub Map 2, Address 0x85[3:0]**

This control provides further contrast enhancement to the luma and chroma gain controls and is particularly effective in the darker areas of an image.

**Table 66. ACE\_GAMMA\_GAIN[3:0] Function**

ACE_GAMMA_GAIN[3:0]	Description
0000	Set further contrast enhancement to minimum value
1000 (default)	Set further contrast enhancements to default value
1111	Set further contrast enhancement to maximum value

**DITHER FUNCTION**

The dither function converts the digital output of the [ADV7182](#) from 8-bit pixel data down to 6-bit pixel data. This function makes it easier for the [ADV7182](#) to communicate with some LCD panels. The dither function is turned off by default. It is activated by the BR\_DITHER\_MODE bit.

**BR\_DITHER\_MODE, User Sub Map 2, Address 0x92[0]****Table 67. BR\_DITHER\_MODE Function**

BR_DITHER_MODE	Description
0 (default)	8-bit to 6-bit down dither disabled
1	8-bit to 6-bit down dither enabled

## AV CODE INSERTION AND CONTROLS

This section describes the I<sup>2</sup>C-based controls that affect the following:

- Insertion of AV codes into the data stream
- Data blanking during the vertical blank interval (VBI)
- The range of data values permitted in the output data stream
- The relative delay of luma vs. chroma signals

### BT.656-4, ITU-R BT.656-3/ITU-R BT.656-4 Enable, Address 0x04[7]

Between Revision 3 and Revision 4 of the ITU-R BT.656 standards, the ITU has changed the toggling position for the V bit within the SAV EAV codes for NTSC. The ITU-R BT.656-4 standard bit allows the user to select an output mode that is compliant with either the ITU-R BT.656-3 standard or ITU-R BT.656-4 standard. For further information, visit the International Telecommunication Union website.

Note that the standard change affects only NTSC and has no bearing on PAL.

When ITU-R BT.656-4 is set to 0 (default), the ITU-R BT.656-3 specification is used. The V bit goes low at EAV of Line 10 and Line 273.

When ITU-R BT.656-4 is 1, the ITU-R BT.656-4 specification is used. The V bit goes low at EAV of Line 20 and Line 283.

### VBI\_EN, Vertical Blanking Interval Data Enable, Address 0x03[7]

The VBI enable bit allows data such as intercast and closed caption data to be passed through the luma channel of the decoder with a minimal amount of filtering. All data for Line 1 to Line 21 is passed through and available at the output port. The ADV7182 does not blank the luma data and automatically switches all filters along the luma data path into their widest bandwidth. For active video, the filter settings for YSH and YPK are restored.

See the BL\_C\_VBI, Blank Chroma During VBI, Address 0x04[2] section for information on the chroma path.

When VBI\_EN is set to 0 (default), all video lines are filtered/scaled.

When VBI\_EN is 1, only the active video region is filtered/scaled.

### BL\_C\_VBI, Blank Chroma During VBI, Address 0x04[2]

Setting BL\_C\_VBI to 1 blanks the Cr and Cb values of all VBI lines. This is done so any data that may arrive during VBI is not decoded as color and is output through Cr and Cb. As a result, it is possible to send VBI lines into the decoder and then output them through an encoder again, undistorted. Without this blanking, any color that is incorrectly decoded is encoded by the video encoder, thus distorting the VBI lines.

Setting BL\_C\_VBI to 0 decodes and outputs color during VBI.

Setting BL\_C\_VBI to 1 (default) blanks Cr and Cb values during VBI.

### Range, Range Selection, Address 0x04[0]

AV codes (as per ITU-R BT.656, formerly known as CCIR-656) consist of a fixed header made up of 0xFF and 0x00 values. These two values are reserved and, therefore, are not to be used for active video. Additionally, the ITU specifies that the nominal range for video should be restricted to values between 16 and 235 for luma and 16 and 240 for chroma.

The range bit allows the user to limit the range of values output by the ADV7182 to the recommended value range. In any case, it ensures that the reserved values of 255d (0xFF) and 00d (0x00) are not presented on the output pins unless they are part of an AV code header.

**Table 68. Range Function**

Range	Description
0	$16 \leq Y \leq 235, 16 \leq C/P \leq 240$
1 (default)	$1 \leq Y \leq 254, 1 \leq C/P \leq 254$

### AUTO\_PDC\_EN, Automatic Programmed Delay Control, Address 0x27[6]

Enabling AUTO\_PDC\_EN activates a function within the ADV7182 that automatically programs the LTA[1:0] and CTA[2:0] registers to have the chroma and luma data match delays for all modes of operation. If AUTO\_PDC\_EN is 1, the LTA[1:0] and CTA[2:0] manual registers are not used. If the automatic mode is disabled (by setting the AUTO\_PDC\_EN bit to 0), the values programmed into the LTA[1:0] and CTA[2:0] registers become active.

When AUTO\_PDC\_EN is set to 0, the ADV7182 uses the LTA[1:0] and CTA[2:0] values for delaying luma and chroma samples. See the LTA[1:0], Luma Timing Adjust, Address 0x27[1:0] section and the CTA[2:0], Chroma Timing Adjust, Address 0x27[5:3] section.

When AUTO\_PDC\_EN is 1 (default), the ADV7182 automatically determines the LTA and CTA values to have luma and chroma aligned at the output.

### LTA[1:0], Luma Timing Adjust, Address 0x27[1:0]

The luma timing adjust bits allow the user to specify a timing difference between chroma and luma samples.

There is a functionality overlap with the CTA[2:0] register. For manual programming, use the following defaults:

- CVBS input LTA[1:0] = 00
- Y/C input LTA[1:0] = 01
- YPrPb input LTA[1:0] = 01

**Table 69. LTA Function**

LTA[1:0]	Description
00 (default)	No delay
01	Luma one clock (37 ns) late
10	Luma two clock (74 ns) early
11	Luma one clock (37 ns) early



**CTA[2:0], Chroma Timing Adjust, Address 0x27[5:3]**

The chroma timing adjust register allows the user to specify a timing difference between chroma and luma samples. This can be used to compensate for external filter group delay differences in the luma vs. chroma path and to allow a different number of pipeline delays while processing the video downstream. Review this functionality together with the LTA[1:0] bits.

The chroma can be delayed or advanced only in chroma pixel steps. One chroma pixel step is equal to two luma pixels. The programmable delay occurs after demodulation, where delay cannot be made by luma pixel steps.

For manual programming, use the following defaults:

- CVBS input CTA[2:0] = 011
- Y/C input CTA[2:0] = 101
- YPrPb input CTA[2:0] = 110

**Table 70. CTA Function**

CTA[2:0]	Description
000	Reserved
001	Chroma + two pixels (early)
010	Chroma + one pixel (early)
011 (default)	No delay
100	Chroma – one pixel (late)
101	Chroma – two pixels (late)
110	Chroma – three pixels (late)
111	Reserved

**SYNCHRONIZATION OUTPUT SIGNALS**

**HSYNC Configuration**

The following controls allow the user to configure the behavior of the HSYNC output signal only:

- Beginning of HSYNC signal via HSB[10:0]
- End of HSYNC signal via HSE[10:0]
- Polarity of HSYNC using PHS

The HSYNC signal can be output on the VS/FIELD/SFL pin or the HS pin (see the Global Pin Control section.)

The HSYNC begin (HSB) and HSYNC end (HSE) registers allow the user to freely position the HSYNC signal within the video line. The values in HSB[10:0] and HSE[10:0] are measured in

**Table 71. HS Timing Parameters**

Standard	Characteristic				
	HS Begin Adjust, HSB[10:0] (Default)	HS End Adjust, HSE[10:0] (Default)	HS to Active Video, LLC Clock Cycles, C in Figure 31 (Default)	Active Video Samples/Line, D in Figure 31	Total LLC Clock Cycles, E in Figure 31
NTSC	0000000010b	0000000000b	272	720Y + 720C = 1440	1716
PAL	0000000010b	0000000000b	284	720Y + 720C = 1440	1728

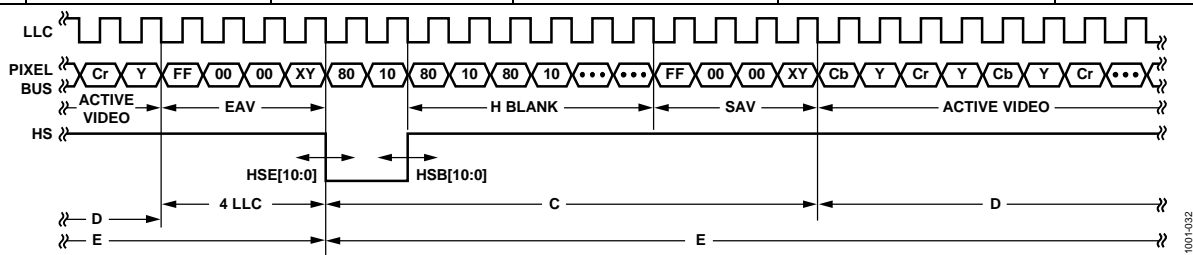


Figure 31. HSYNC Timing  
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pixel units from the falling edge of HSYNC. Using both values, the user can program both the position and length of the HSYNC output signal.

**HSB[10:0], HSYNC Begin, Address 0x34[6:4], Address 0x35[7:0]**

The position of this edge is controlled by placing a binary number into HSB[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV Code FF, 00, 00, XY (see Figure 31). HSB is set to 0000000010b, which is two LLC clock cycles from count [0].

The default value of HSB[10:0] is 0x02, indicating that the HSYNC pulse starts two pixels after the falling edge of HSYNC.

**HSE[10:0], HSYNC End, Address 0x34[2:0], Address 0x36[7:0]**

The position of this edge is controlled by placing a binary number into HSE[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV Code FF, 00, 00, XY (see Figure 31). HSE is set to 0000000000b, which is 0 LLC clock cycles from count [0].

The default value of HSE[10:0] is 00, indicating that the HSYNC pulse ends 0 pixels after the falling edge of HSYNC.

For example,

- To shift the HSYNC toward active video by 20 LLCs, add 20 LLCs to both HSB and HSE, that is, HSB[10:0] = [0000010110], HSE[10:0] = [0000010100].
- To shift the HSYNC away from active video by 20 LLCs, add 1696 LLCs to both HSB and HSE (for NTSC), that is, HSB[10:0] = [11010100010], HSE[10:0] = [11010100000]. Therefore, 1696 is derived from the NTSC total number of pixels, 1716.
- To move 20 LLCs away from active video, subtract 20 from 1716 and add the result in binary to both HSB[10:0] and HSE[10:0].

**PHS, HSYNC Polarity, Address 0x37[7]**

The polarity of the HSYNC signal can be inverted using the PHS bit.

When PHS is 0 (default), HSYNC is active low.

When PHS is 1, HSYNC is active high.

**VSYNC and FIELD Configuration**

The following controls allow the user to configure the behavior of the VSYNC and FIELD output signals, as well as the generation of embedded AV codes. Note that the VSYNC and FIELD signals can be output on the VS/FIELD/SFL pin or the HS pin (see the Global Pin Control section).

**NEWAVMODE, New AV Mode, Address 0x31[4]**

When NEWAVMODE is 0, EAV/SAV codes are generated to suit Analog Devices encoders. No adjustments are possible.

When NEWAVMODE is 1 (default), it enables the manual position of the VSYNC, FIELD, and AV codes using Register 0x32 to Register 0x33 and Register 0xE5 to Register 0xEA. Default register settings are CCIR656 (BT.565-4) compliant; see Figure 32, Figure 33 for NTSC and Figure 37, Figure 38 for PAL

**HVSTIM, Horizontal VSYNC Timing, Address 0x31[3]**

The HVSTIM bit allows the user to select where the VSYNC signal is asserted within a line of video. Some interface circuitry may require VSYNC to go low while HSYNC is low.

When HVSTIM is 0 (default), the start of the line is relative to HSE.

When HVSTIM is 1, the start of the line is relative to HSB.

**VSBHO, VSYNC Begin Horizontal Position Odd, Address 0x32[7]**

The VSBHO and VSBHE bits select the position within a line at which the VSYNC signal (not the bit in the AV code) becomes active. Some follow-on chips require the VSYNC signal to change state only when HSYNC is high or low.

When VSBHO is 0 (default), the VSYNC signal goes high in the middle of a line of video (odd field).

When VSBHO is 1, the VSYNC signal changes state at the start of a line (odd field).

**VSBHE, VSYNC Begin Horizontal Position Even, Address 0x32[6]**

The VSBHO and VSBHE bits select the position within a line at which the VSYNC signal (not the bit in the AV code) becomes active. Some follow-on chips require the VSYNC signal to change state only when HS is high or low.

When VSBHE is 0 (default), the VSYNC signal goes high in the middle of a line of video (even field).

When VSBHE is 1, the VSYNC signal changes state at the start of a line (even field).

**VSEHO, VSYNC End Horizontal Position Odd, Address 0x33[7]**

The VSEHO and VSEHE bits select the position within a line at which the VSYNC signal (not the bit in the AV code) becomes active. Some follow-on chips require the VSYNC signal to change state only when HSYNC is high or low.

When VSEHO is 0 (default), the VSYNC signal goes low (inactive) in the middle of a line of video (odd field).

When VSEHO is 1, the VSYNC signal changes state at the start of a line (odd field).

**VSEHE, VSYNC End Horizontal Position Even, Address 0x33[6]**

The VSEHO and VSEHE bits select the position within a line at which the VSYNC signal (not the bit in the AV code) becomes active. Some follow-on chips require the VSYNC signal to change state only when HS is high or low.

When VSEHE is 0 (default), the VSYNC signal goes low (inactive) in the middle of a line of video (even field).

When VSEHE is 1, the VSYNC signal changes state at the start of a line (even field).

**PVS, VSYNC Polarity, Address 0x37[5]**

The polarity of the VSYNC signal can be inverted using the PVS bit.

When PVS is 0 (default), VSYNC is active high.

When PVS is 1, VSYNC is active low.

**PF, FIELD Polarity, Address 0x37[3]**

The FIELD pin can be inverted using the PHS bit.

When PHS is 0 (default), FIELD pin is active high.

When PHS is 1, FIELD pin is active low.

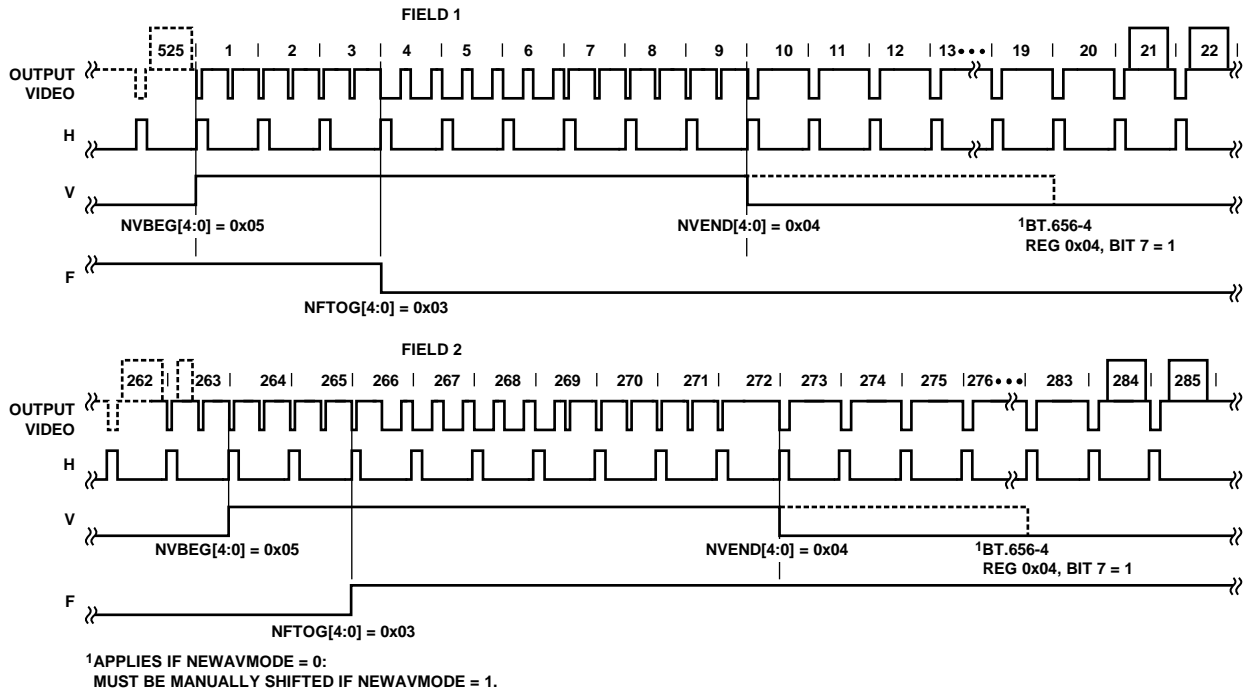


Figure 32. NTSC Default, ITU-R BT.656 (Polarity of H, V, and F Embedded in Data)

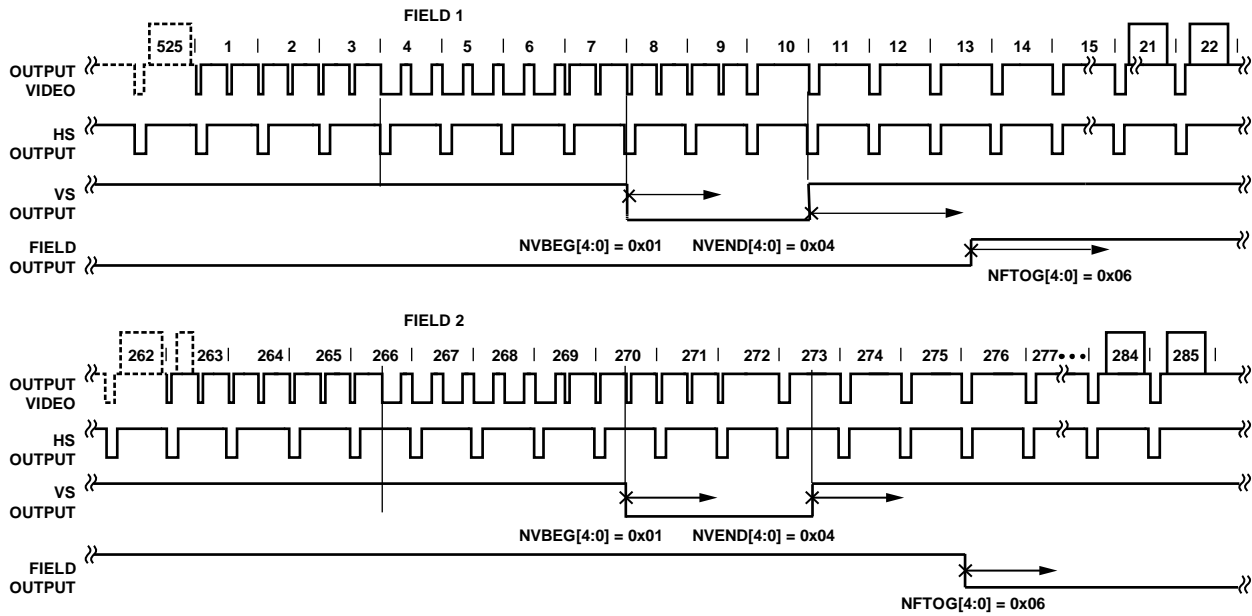


Figure 33. NTSC Typical VS/FIELD Positions

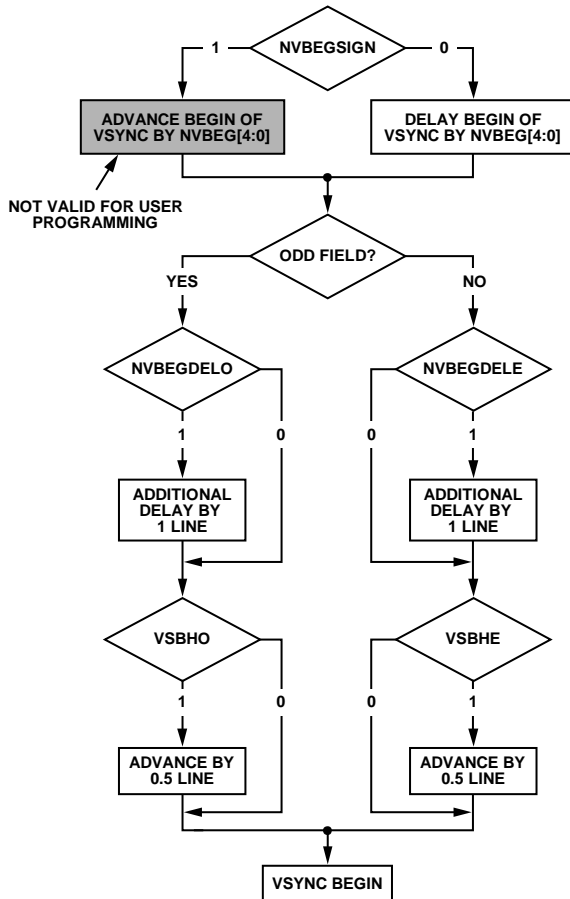


Figure 34. NTSC VSYNC Begin

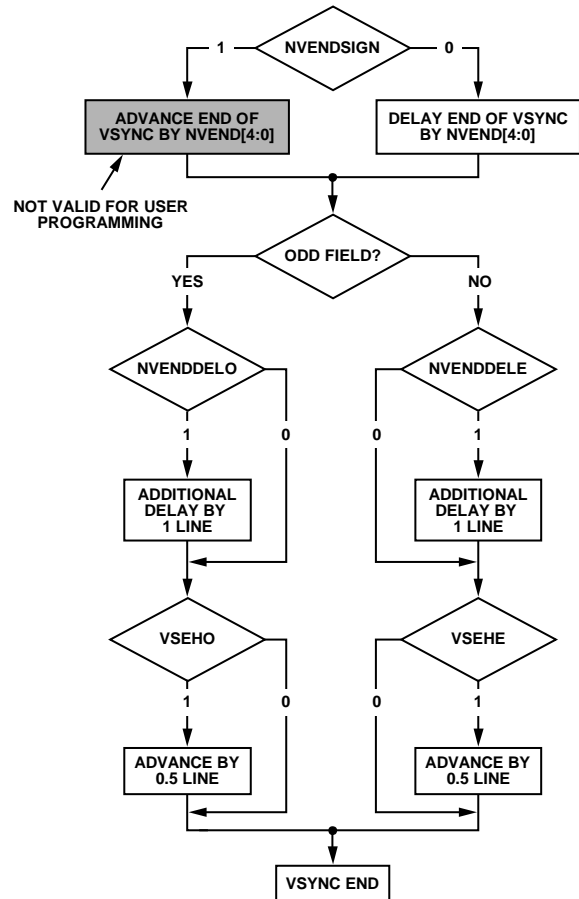


Figure 35. NTSC VSYNC End

**NVBEGDELO, NTSC VSYNC Begin Delay on Odd Field, Address 0xE5[7]**

When NVBEGDELO is 0 (default), there is no delay.  
 Setting NVBEGDELO to 1 delays VSYNC going high by one line relative to NVBEG (odd field).

**NVBEGDELE, NTSC VSYNC Begin Delay on Even Field, Address 0xE5[6]**

When NVBEGDELE is 0 (default), there is no delay.  
 Setting NVBEGDELE to 1 delays VSYNC going high by one line relative to NVBEG (even field).

**NVBEGSIGN, NTSC VSYNC Begin Sign, Address 0xE5[5]**

Setting NVBEGSIGN to 0 delays the start of VSYNC; sets to low when manual programming.  
 Setting NVBEGSIGN to 1 (default) advances the start of VSYNC; however, it is not suitable for user programming.

**NVBEG[4:0], NTSC VSYNC Begin, Address 0xE5[4:0]**

The default value of NVBEG is 00101, indicating the NTSC VSYNC begin position. For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC signal are modified.

**NVENDDELO, NTSC VSYNC End Delay on Odd Field, Address 0xE6[7]**

When NVENDDELO is 0 (default), there is no delay.  
 Setting NVENDDELO to 1 delays VSYNC going low by one line relative to NVEND (odd field).

**NVENDDELE, NTSC VSYNC End Delay on Even Field, Address 0xE6[6]**

When NVENDDELE is 0 (default), there is no delay.  
 Setting NVENDDELE to 1 delays VSYNC going low by a line relative to NVEND (even field).

**NVENDSIGN, NTSC VSYNC End Sign, Address 0xE6[5]**

Setting NVENDSIGN to 0 (default) delays the end of VSYNC; sets to low when manual programming.  
 Setting NVENDSIGN to 1 advances the end of VSYNC; however, it is not suitable for user programming.

**NVEND[4:0], NTSC VSYNC End, Address 0xE6[4:0]**

The default value of NVEND is 00100, indicating the NTSC VSYNC end position.  
 For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC signal are modified.

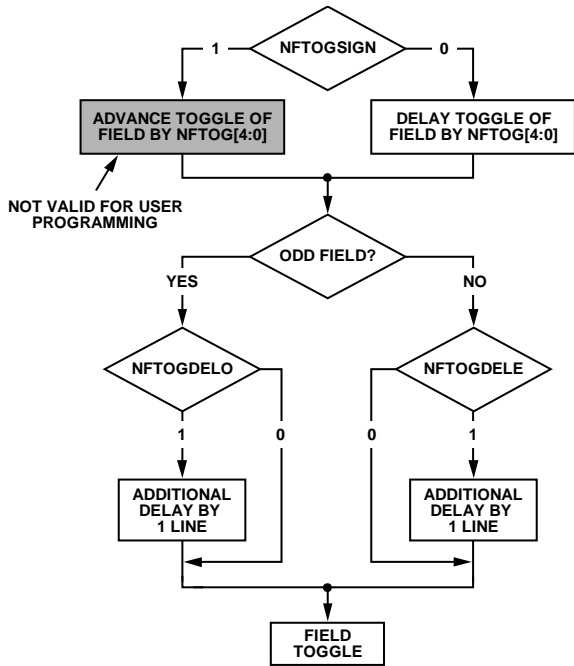


Figure 36. NTSC FIELD Toggle

11001-037

**NFTOGDELO, NTSC FIELD Toggle Delay on Odd Field, Address 0xE7[7]**

When NFTOGDELO is 0 (default), there is no delay.

Setting NFTOGDELO to 1 delays the FIELD toggle/transition by one line relative to NFTOG (odd field).

**NFTOGDELE, NTSC FIELD Toggle Delay on Even Field, Address 0xE7[6]**

When NFTOGDELE is 0, there is no delay.

Setting NFTOGDELE to 1 (default) delays the FIELD toggle/transition by one line relative to NFTOG (even field).

**NFTOGSIGN, NTSC FIELD Toggle Sign, Address 0xE7[5]**

Setting NFTOGSIGN to 0 delays the FIELD toggle/transition; sets to low when manual programming.

Setting NFTOGSIGN to 1 (default) advances the FIELD toggle/transition; however, it is not suitable for user programming.

**NFTOG[4:0], NTSC FIELD Toggle, Address 0xE7[4:0]**

The default value of NFTOG is 00011, indicating the NTSC field toggle position.

For all NTSC/PAL field timing controls, both the F bit in the AV code and the field signal are modified.

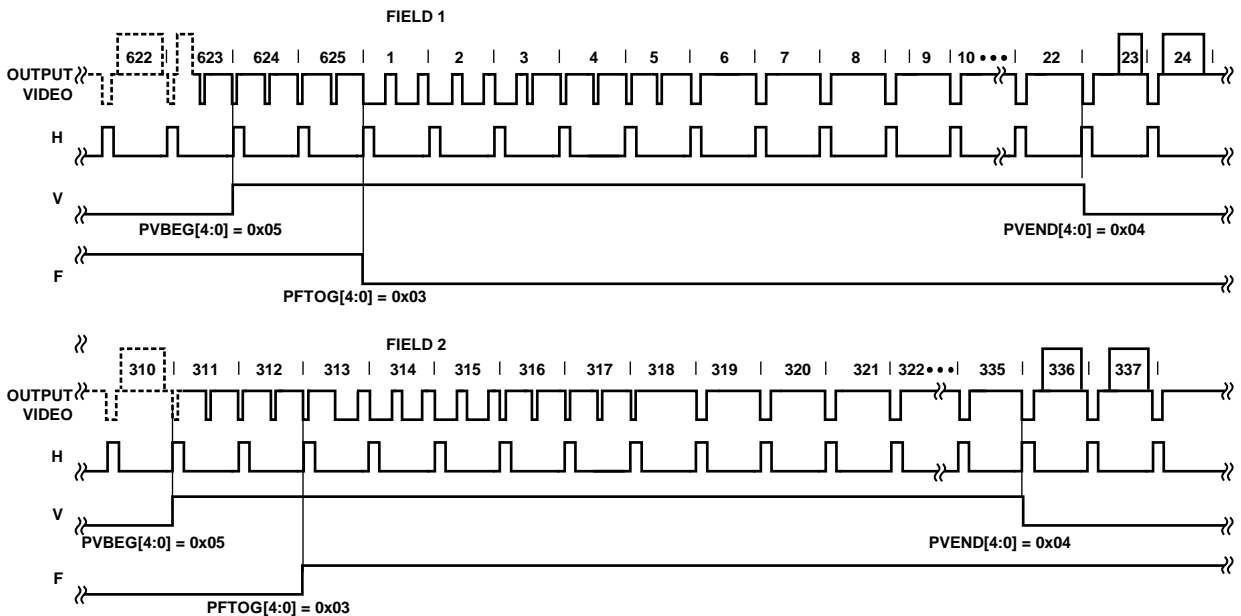


Figure 37. PAL Default, ITU-R BT.656 (Polarity of H, V, and F Embedded in Data)

11001-038

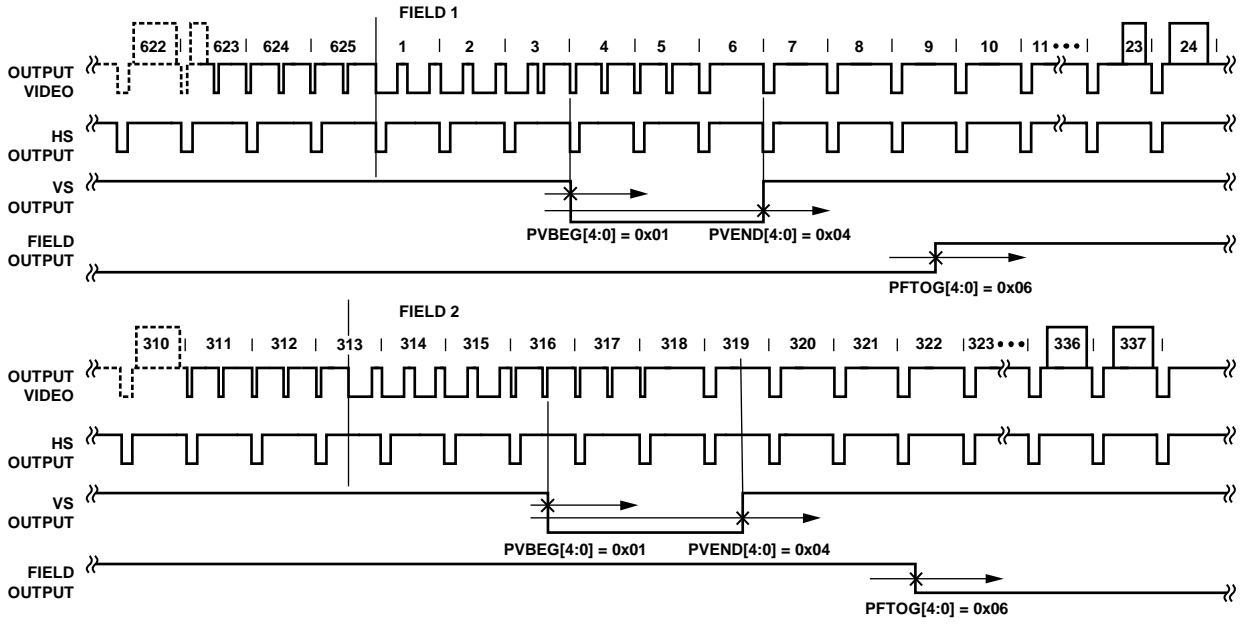


Figure 38. PAL Typical VS/FIELD Positions

11001-039

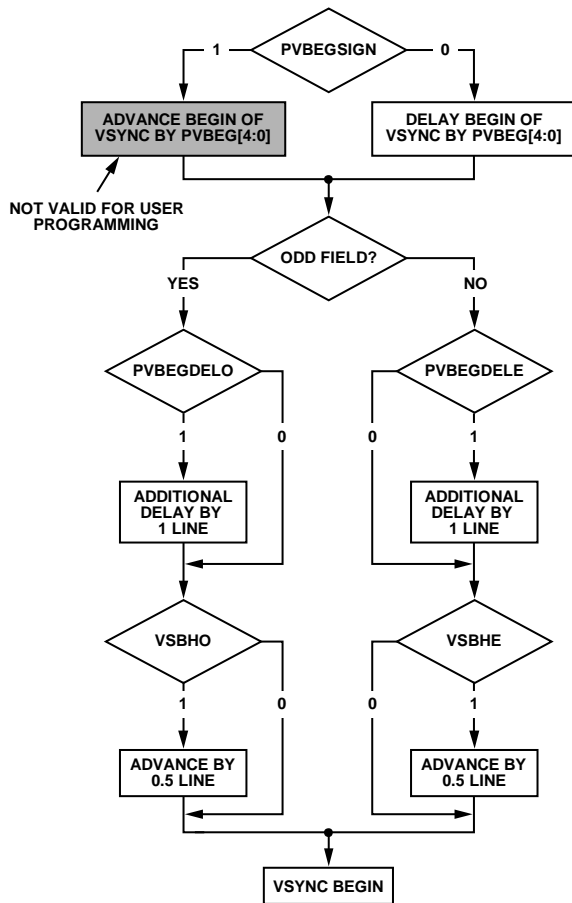


Figure 39. PAL VSYNC Begin

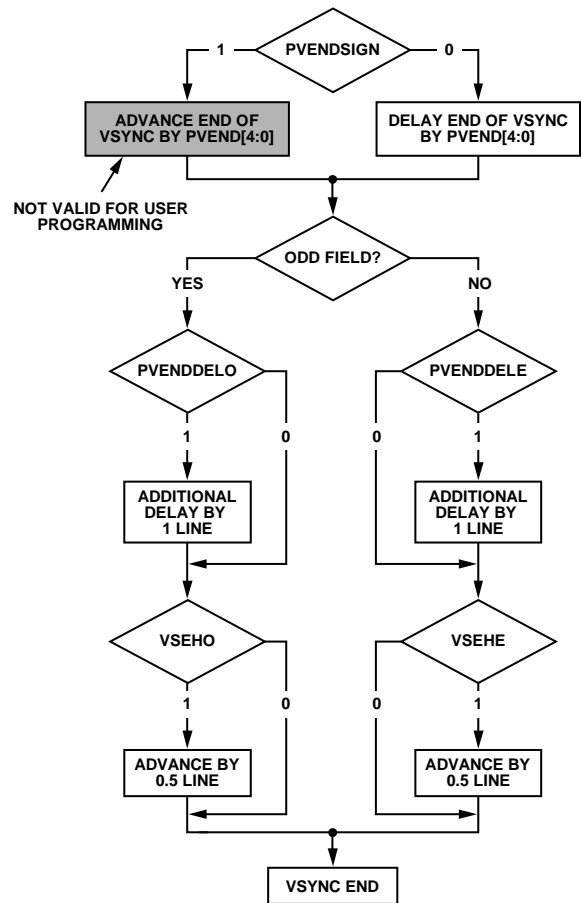


Figure 40. PAL VSYNC End

**PVBEGDELO, PAL VSYNC Begin Delay on Odd Field, Address 0xE8[7]**

When PVBEGDELO is 0 (default), there is no delay.  
 Setting PVBEGDELO to 1 delays VSYNC going high by one line relative to PVBEG (odd field).

**PVBEGDELE, PAL VSYNC Begin Delay on Even Field, Address 0xE8[6]**

When PVBEGDELE is 0, there is no delay.  
 Setting PVBEGDELE to 1 (default) delays VSYNC going high by one line relative to PVBEG (even field).

**PVBEGSIGN, PAL VSYNC Begin Sign, Address 0xE8[5]**

Setting PVBEGSIGN to 0 delays the beginning of VSYNC; sets to low when manual programming.  
 Setting PVBEGSIGN to 1 (default) advances the beginning of VSYNC; however, it is not suitable for user programming.

**PVBEG[4:0], PAL VSYNC Begin, Address 0xE8[4:0]**

The default value of PVBEG is 00101, indicating the PAL VSYNC begin position. For all NTSC/PAL VSYNC timing controls, the V bit in the AV code and the VSYNC signal are modified.

**PVENDELO, PAL VSYNC End Delay on Odd Field, Address 0xE9[7]**

When PVENDELO is 0 (default), there is no delay.  
 Setting PVENDELO to 1 delays VSYNC going low by one line relative to PVEND (odd field).

**PVENDELE, PAL VSYNC End Delay on Even Field, Address 0xE9[6]**

When PVENDELE is 0 (default), there is no delay.  
 Setting PVENDELE to 1 delays VSYNC going low by one line relative to PVEND (even field).

**PVENDSIGN, PAL VSYNC End Sign, Address 0xE9[5]**

Setting PVENDSIGN to 0 (default) delays the end of VSYNC; sets to low when manual programming.  
 Setting PVENDSIGN to 1 advances the end of VSYNC ; however, it is not suitable for user programming.

**PVEND[4:0], PAL VSYNC End, Address 0xE9[4:0]**

The default value of PVEND is 10100, indicating the PAL VSYNC end position.  
 For all NTSC/PAL VSYNC timing controls, both the V bit in the AV code and the VSYNC signal are modified.

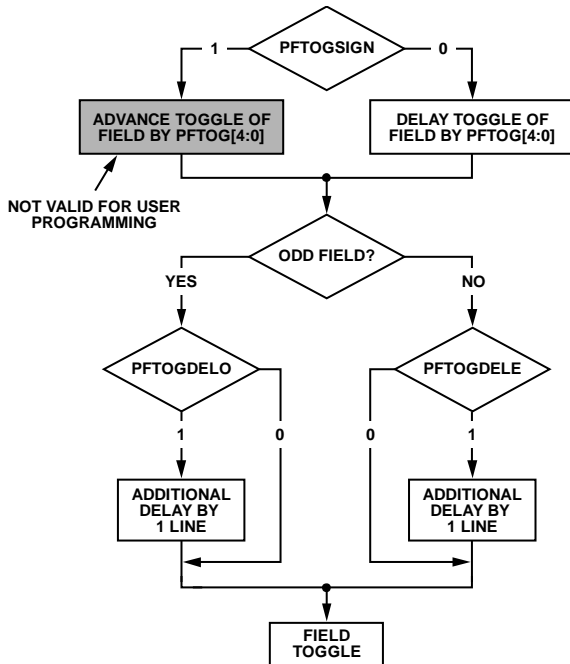


Figure 41. PAL FIELD Toggle

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**PFTOGDELO, PAL FIELD Toggle Delay on Odd Field, Address 0xEA[7]**

When PFTOGDELO is 0 (default), there is no delay.  
 Setting PFTOGDELO to 1 delays the FIELD toggle/transition by one line relative to PFTOG (odd field).

**PFTOGDELE, PAL FIELD Toggle Delay on Even Field, Address 0xEA[6]**

When PFTOGDELE is 0, there is no delay.  
 Setting PFTOGDELE to 1 (default) delays the FIELD toggle/transition by one line relative to PFTOG (even field).

**PFTOGSIGN, PAL FIELD Toggle Sign, Address 0xEA[5]**

Setting PFTOGSIGN to 0 delays the field transition and set to low when manual programming.  
 Setting PFTOGSIGN to 1 (default) advances the field transition; however, it is not suitable for user programming.

**PFTOG, PAL FIELD Toggle, Address 0xEA[4:0]**

The default value of PFTOG is 00011, indicating the PAL field toggle position.

For all NTSC/PAL field timing controls, the F bit in the AV code and the FIELD signal are modified.

**SYNC PROCESSING**

The ADV7182 has two additional sync processing blocks that postprocess the raw synchronization information extracted from the digitized input video. If desired, the blocks can be disabled via the following two I<sup>2</sup>C bits: ENHSPLL and ENVSPROC.

**ENHSPLL, Enable HSYNC Processor, Address 0x01[6]**

The HSYNC processor is designed to filter incoming HSYNCS that have been corrupted by noise, providing improved performance for video signals with stable time bases but poor SNR.

Setting ENHSPLL to 0 disables the HSYNC processor.

Setting ENHSPLL to 1 (default) enables the HSYNC processor.

**ENVSPROC, Enable VSYNC Processor, Address 0x01[3]**

This block provides extra filtering of the detected VSYNCS to improve vertical lock.

Setting ENVSPROC to 0 disables the VSYNC processor.

Setting ENVSPROC to 1 (default) enables the VSYNC processor.

**VBI DATA DECODE**

The VBI data processor (VDP) on the ADV7182 can slice both low bandwidth standards and high bandwidth standards such as teletext.

The VDP is capable of slicing multiple VBI data standards on SD video. It decodes the VBI data on the incoming CVBS and Y/C or YUV data. The decoded results are available as ancillary data in output 656 data stream. For low data rate VBI standards like CC/WSS/CGMS, the decoded data bytes can be read from the I<sup>2</sup>C registers.

The VBI data standards that can be decoded by the VDP are listed in Table 72 and Table 73.

Table 72. PAL

Feature	Standard
Teletext System A, Teletext System C, or Teletext System D	ITU-R BT.653
Teletext System B/ Teletext System WST	ITU-R BT.653
Wide Screen Signaling (WSS)	ITU-R BT.1119-1/ ETSI EN.300294
Closed Captioning (CCAP)	Not applicable

Table 73. NTSC

Feature	Standard
Teletext System B and Teletext System D	ITU-R BT.653
Teletext System C/ Teletext System NABTS	ITU-R BT.653/ EIA-516
Copy Generation Management System (CGMS)	EIA-J CPR-1204/ IEC 61880
Closed Captioning (CCAP)	EIA-608



The VBI data standard that the VDP decodes on a particular line of incoming video has been set by default as described in Table 74. This can be overridden manually and any VBI data can be decoded on any line. The details of manual programming are described in Table 75.

**VDP Default Configuration**

The VDP can decode different VBI data standards on a line-to-line basis. The various standards supported by default on different lines of VBI are explained in Table 74.

**VDP Manual Configuration**

**MAN\_LINE\_PGM, Enable Manual Line Programming of VBI Standards, Address 0x64[7], Interrupt/VDP Map**

The user can configure the VDP to decode different standards on a line-to-line basis through manual line programming. For this, set the MAN\_LINE\_PGM bit. The user must write into all the line programming registers, VBI\_DATA\_Px\_Ny and VBI\_DATA\_Px (see Register 0x64 to Register 0x77 in Table 96).

When MAN\_LINE\_PGM is set to 0 (default), the VDP decodes default standards on lines, as shown in Table 74.

When MAN\_LINE\_PGM is set to 1, the VBI standards to be decoded are manually programmed.

**VBI\_DATA\_Px\_Ny[3:0], VBI\_DATA\_Px[3:0], VBI Standard to be Decoded on Line X for PAL, Line Y for NTSC, Address 0x64 to Address 0x77, Interrupt/VDP Map**

These are related 4-bit clusters in Register 0x64 to Register 0x77 of the Interrupt/VDP Map Details (see Table 93). These 4-bit, line programming registers, VBI\_DATA\_Px\_Ny and VBI\_DATA\_Px, identify the VBI data standard that is decoded on Line X in PAL mode or on Line Y in NTSC mode. The different types of VBI standards decoded by VBI\_DATA\_Px\_Ny and VBI\_DATA\_Px are shown in Table 75. Note that the X or Y value depends on whether the ADV7182 is in PAL or NTSC mode.

**Table 74. Default Standards on Lines for PAL and NTSC**

PAL—625/50				NTSC—525/60			
Line No.	Default VBI Data Decoded	Line No.	Default VBI Data Decoded	Line No.	Default VBI Data Decoded	Line No.	Default VBI Data Decoded
6	WST	318	Reserved	23	Reserved	286	Reserved
7	WST	319	WST	24	Reserved	287	Reserved
8	WST	320	WST	25	Reserved	288	Reserved
9	WST	321	WST	10	NABTS	272	NABTS
10	WST	322	WST	11	NABTS	273	NABTS
11	WST	323	WST	12	NABTS	274	NABTS
12	WST	324	WST	13	NABTS	275	NABTS
13	WST	325	WST	14	Reserved	276	NABTS
14	WST	326	WST	15	NABTS	277	Reserved
15	WST	327	WST	16	Reserved	278	NABTS
16	Reserved	328	WST	17	NABTS	279	Reserved
17	Reserved	329	Reserved	18	NABTS	280	NABTS
18	Reserved	332	Reserved	19	NABTS	281	NABTS
19	Reserved	333	WST	20	CGMS	282	NABTS
20	WST	334	WST	21	CCAP	283	CGMS
21	WST	335	CCAP	22 + full odd field	NABTS	284	CCAP
22	CCAP	336	WST	Reserved	Reserved	285 + full even field	NABTS
23	WSS	337 + full even field	WST	Reserved	Reserved	Reserved	Reserved
24 + full odd field	WST	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

**Table 75. VBI Data Standards for Manual Configuration**

VBI_DATA_Px_Ny	PAL—625/50	NTSC—525/60
0000	Disable VDP	Disable VDP
0001	Teletext system identified by VDP_TTXT_TYPE	Teletext system identified by VDP_TTXT_TYPE
0010	Reserved	Reserved
0011	Reserved	Reserved
0100	WSS ITU-R BT.1119-1/ETSI.EN.300294	CGMS EIA-J CPR-1204/IEC 61880
0101	Reserved	Reserved
0110	Reserved	Reserved
0111	CCAP	CCAP EIA-608
1000 to 1111	Reserved	Reserved

Table 76.VBI Data Standards to be Decoded on Line Px (PAL) or Line Ny (NTSC)

Signal Name	Bit Location	Dec Address	Hex Address
VBI_DATA_P6_N23	VDP_LINE_00F[7:4]	101	0x65
VBI_DATA_P7_N24	VDP_LINE_010[7:4]	102	0x66
VBI_DATA_P8_N25	VDP_LINE_011[7:4]	103	0x67
VBI_DATA_P9	VDP_LINE_012[7:4]	104	0x68
VBI_DATA_P10	VDP_LINE_013[7:4]	105	0x69
VBI_DATA_P11	VDP_LINE_014[7:4]	106	0x6A
VBI_DATA_P12_N10	VDP_LINE_015[7:4]	107	0x6B
VBI_DATA_P13_N11	VDP_LINE_016[7:4]	108	0x6C
VBI_DATA_P14_N12	VDP_LINE_017[7:4]	109	0x6D
VBI_DATA_P15_N13	VDP_LINE_018[7:4]	110	0x6E
VBI_DATA_P16_N14	VDP_LINE_019[7:4]	111	0x6F
VBI_DATA_P17_N15	VDP_LINE_01A[7:4]	112	0x70
VBI_DATA_P18_N16	VDP_LINE_01B[7:4]	113	0x71
VBI_DATA_P19_N17	VDP_LINE_01C[7:4]	114	0x72
VBI_DATA_P20_N18	VDP_LINE_01D[7:4]	115	0x73
VBI_DATA_P21_N19	VDP_LINE_01E[7:4]	116	0x74
VBI_DATA_P22_N20	VDP_LINE_01F[7:4]	117	0x75
VBI_DATA_P23_N21	VDP_LINE_020[7:4]	118	0x76
VBI_DATA_P24_N22	VDP_LINE_021[7:4]	119	0x77
VBI_DATA_P318	VDP_LINE_00E[3:0]	100	0x64
VBI_DATA_P319_N286	VDP_LINE_00F[3:0]	101	0x65
VBI_DATA_P320_N287	VDP_LINE_010[3:0]	102	0x66
VBI_DATA_P321_N288	VDP_LINE_011[3:0]	103	0x67
VBI_DATA_P322	VDP_LINE_012[3:0]	104	0x68
VBI_DATA_P323	VDP_LINE_013[3:0]	105	0x69
VBI_DATA_P324_N272	VDP_LINE_014[3:0]	106	0x6A
VBI_DATA_P325_N273	VDP_LINE_015[3:0]	107	0x6B
VBI_DATA_P326_N274	VDP_LINE_016[3:0]	108	0x6C
VBI_DATA_P327_N275	VDP_LINE_017[3:0]	109	0x6D
VBI_DATA_P328_N276	VDP_LINE_018[3:0]	110	0x6E
VBI_DATA_P329_N277	VDP_LINE_019[3:0]	111	0x6F
VBI_DATA_P330_N278	VDP_LINE_01A[3:0]	112	0x70
VBI_DATA_P331_N279	VDP_LINE_01B[3:0]	113	0x71
VBI_DATA_P332_N280	VDP_LINE_01C[3:0]	114	0x72
VBI_DATA_P333_N281	VDP_LINE_01D[3:0]	115	0x73
VBI_DATA_P334_N282	VDP_LINE_01E[3:0]	116	0x74
VBI_DATA_P335_N283	VDP_LINE_01F[3:0]	117	0x75
VBI_DATA_P336_N284	VDP_LINE_020[3:0]	118	0x76
VBI_DATA_P337_N285	VDP_LINE_021[3:0]	119	0x77

Full field detection (lines other than VBI lines) of any standard can also be enabled by writing to the VBI\_DATA\_P24\_N22[3:0] and VBI\_DATA\_P337\_N285[3:0] bits. So, if VBI\_DATA\_P24\_N22[3:0] is programmed with any teletext standard, teletext is decoded off for the entire odd field. The corresponding register for the even field is VBI\_DATA\_P337\_N285[3:0].

For teletext system identification, VDP assumes that if teletext is present in a video channel, all the teletext lines comply with a single standard system. Therefore, the line programming using the VBI\_DATA\_Px\_Ny and VBI\_DATA\_Px registers identifies whether the data in line is teletext; the actual standard is identified by the VDP\_TTXX\_TYPE\_MAN bit.

To program the VDP\_TTXX\_TYPE\_MAN bit, the VDP\_TTXX\_TYPE\_MAN\_ENABLE bit must be set to 1.

**VDP\_TTXX\_TYPE\_MAN\_ENABLE, Enable Manual Selection of Teletext Type, Address 0x60[2], Interrupt/VDP Map**

Setting VDP\_TTXX\_TYPE\_MAN\_ENABLE to 0 (default), disables manual programming of the teletext type.

Setting VDP\_TTXX\_TYPE\_MAN\_ENABLE to 1, enables manual programming of the teletext type.

**VDP\_TTXT\_TYPE\_MAN[1:0], Specify the Teletext Type, Address 0x60[1:0], Interrupt/VDP Map**

These bits specify the teletext type to be decoded. These bits are functional only if VDP\_TTXT\_TYPE\_MAN\_ENABLE is set to 1.

**Table 77. VDP\_TTXT\_TYPE\_MAN Function**

VDP_TTXT_TYPE_MAN[1:0]	625/50 (PAL)	525/60 (NTSC)
00 (default)	Teletext-ITU-BT.653-625/50-A	Reserved
01	Teletext-ITU-BT.653-625/50-B (WST)	Teletext-ITU-BT.653-525/60-B
10	Teletext-ITU-BT.653-625/50-C	Teletext-ITU-BT.653-525/60-C or EIA516 (NABTS)
11	Teletext-ITU-BT.653-625/50-D	Teletext-ITU-BT.653-525/60-D

**VDP Ancillary Data Output**

Reading the data back via I<sup>2</sup>C may not be feasible for VBI data standards with high data rates (for example, teletext). An alternative is to place the sliced data in a packet in the line blanking of the digital output CCIR656 stream. This is available for all standards sliced by the VDP module.

When data is sliced on a given line, the corresponding ancillary data packet is placed immediately after the next EAV code that occurs at the output (that is, data sliced from multiple lines are not buffered up and then emitted in a burst). Note that, due to the vertical delay through the comb filters, the line number on which the packet is placed differs from the line number on which the data was sliced.

The user can enable or disable the insertion of VDP results that have been decoded into the 656 ancillary streams by using the ADF\_ENABLE bit.

**ADF\_ENABLE, Enable Ancillary Data Output Through 656 Stream, Address 0x62[7], User Sub Map 2**

Setting ADF\_ENABLE to 0 (default) disables the insertion of VBI decoded data into the ancillary 656 stream.

Setting ADF\_ENABLE to 1 enables the insertion of VBI decoded data into the ancillary 656 stream.

The user may select the data identification word (DID) and the secondary data identification word (SDID) through programming the ADF\_DID[4:0] and ADF\_SDID[5:0] bits, respectively.

**ADF\_DID[4:0], User-Specified Data ID Word in Ancillary Data, Address 0x62[4:0], Interrupt/VDP Map**

These bits select the data ID word to be inserted into the ancillary data stream with the data decoded by the VDP.

The default value of ADF\_DID[4:0] is 10101.

**ADF\_SDID[5:0], User-Specified Secondary Data ID Word in Ancillary Data, Address 0x63[5:0], Interrupt/VDP Map**

These bits select the secondary data ID word to be inserted in the ancillary data stream with the data decoded by the VDP.

The default value of ADF\_SDID[5:0] is 101010.

**DUPLICATE\_ADF, Enable Duplication/Spreading of Ancillary Data over Y and C Buses, Address 0x63[7], Interrupt/VDP Map**

This bit determines whether the ancillary data is duplicated over both Y and C buses or if the data packets are spread between the two channels.

When DUPLICATE\_ADF to 0 (default) is set, the ancillary data packet is spread across the Y and C data streams.

When DUPLICATE\_ADF to 1 is set, the ancillary data packet is duplicated on the Y and C data streams.

**ADF\_MODE[1:0], Determine the Ancillary Data Output Mode, Address 0x62[6:5], Interrupt/VDP Map**

These bits determine whether the ancillary data output mode is in byte mode or nibble mode.

**Table 78. ADF\_MODE**

ADF_MODE[1:0]	Description
00 (default)	Nibble mode
01	Byte mode, no code restrictions
10	Byte mode, but 0x00 and 0xFF prevented (0x00 replaced by 0x01, 0xFF replaced by 0xFE)
11	Reserved

The ancillary data packet sequence is explained in Table 79 and Table 80. The nibble output mode is the default mode of output from the ancillary stream when ancillary stream output is enabled. This format is in compliance with ITU-R BT.1364.

The following abbreviations are used in Table 79 and Table 80:

- EP—Even parity for Bit B8 to Bit B2. The parity bit's EP is set so that an even number of 1s are in Bit B8 to Bit B2, including the parity bit, B8.
- CS—Checksum word. The CS word is used to increase confidence of the integrity of the ancillary data packet from the DID, SDID, and dc through user data-words (UDWs). It consists of 10 bits that include the following: a 9-bit calculated value and B9 as the inverse of B8. The checksum value B8 to B0 is equal to the nine LSBs of the sum of the nine LSBs of the DID, SDID, and dc, and all UDWs in the packet. Prior to the start of the checksum count cycle, all checksum and carry bits are preset to 0. Any carry resulting from the checksum count cycle is ignored.

- $\overline{EP}$ —The MSB, B9, is the inverse of EP. This ensures that restricted Code 0x00 and Code 0xFF do not occur.
- LINE\_NUMBER[9:0]—The line number of the line that immediately precedes the ancillary data packet. The line number is from the numbering system in ITU-R BT.470. The line number runs from 1 to 625 in a 625-line system and from 1 to 263 in a 525-line system. Note that, due to the vertical delay through the comb filters, the line number on which the packet is output differs from the line number on which the VBI data was sliced.
- Data count—The data count specifies the number of UDWs in the ancillary stream for the standard. The total number of user data-words is four times the data count. Padding words can be introduced to make the total number of UDWs divisible by 4.

Table 79. Ancillary Data in Nibble Output Format

Byte	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Description	
0	0	0	0	0	0	0	0	0	0	0	Ancillary data preamble	
1	1	1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1	1	1		
3	$\overline{EP}$	EP	0	I <sup>2</sup> C_DID6_2[4:0]				0	0	0	DID (data identification word)	
4	$\overline{EP}$	EP	I <sup>2</sup> C_SDID7_2[5:0]				0	0	0	0	SDID (secondary data identification word)	
5	$\overline{EP}$	EP	0	DC[4:0]				0	0	0	Data count	
6	$\overline{EP}$	EP	Padding[1:0]		VBI_DATA_STD[3:0]			0	0	0	ID0 (User Data-Word 1)	
7	$\overline{EP}$	EP	0	LINE_NUMBER[9:5]				0	0	0	ID1 (User Data-Word 2)	
8	$\overline{EP}$	EP	EVEN_FIELD	LINE_NUMBER[4:0]				0	0	0	ID2 (User Data-Word 3)	
9	$\overline{EP}$	EP	0	0	0	0	VDP_TTX_TTYPE[1:0]	0	0	0	ID3 (User Data-Word 4)	
10	$\overline{EP}$	EP	0	0	VBI_WORD_1[7:4]			0	0	0	ID4 (User Data-Word 5)	
11	$\overline{EP}$	EP	0	0	VBI_WORD_1[3:0]			0	0	0	ID5 (User Data-Word 6)	
12	$\overline{EP}$	EP	0	0	VBI_WORD_2[7:4]			0	0	0	ID6 (User Data-Word 7)	
13	$\overline{EP}$	EP	0	0	VBI_WORD_2[3:0]			0	0	0	ID7 (User Data-Word 8)	
14	$\overline{EP}$	EP	0	0	VBI_WORD_3[7:4]			0	0	0	ID8 (User Data-Word 9)	
											Pad 0x200; these padding words may be present, depending on ancillary data type; user data-word	
n - 3	1	0	0	0	0	0	0	0	0	0		
n - 2	1	0	0	0	0	0	0	0	0	0		
n - 1	$\overline{B8}$	Checksum (CS)							0	0	0	CS (checksum word)

Table 80. Ancillary Data in Byte Output Format<sup>1</sup>

Byte	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	Description	
0	0	0	0	0	0	0	0	0	0	0	Ancillary data preamble	
1	1	1	1	1	1	1	1	1	1	1		
2	1	1	1	1	1	1	1	1	1	1		
3	EP	EP	0	I <sup>2</sup> C_DID6_2[4:0]					0	0		DID
4	EP	EP	I <sup>2</sup> C_SDID7_2[5:0]					0	0			SDID
5	EP	EP	0	DC[4:0]					0	0		Data count
6	EP	EP	Padding[1:0]		VBI_DATA_STD[3:0]			0	0			ID0 (User Data-Word 1)
7	EP	EP	0	LINE_NUMBER[9:5]				0	0			ID1 (User Data-Word 2)
8	EP	EP	EVEN_FIELD	LINE_NUMBER[4:0]			0	0				ID2 (User Data-Word 3)
9	EP	EP	0	0	0	0	VDP_TTXT_TYPE[1:0]		0	0		ID3 (User Data-Word 4)
10	VBI_WORD_1[7:0]							0	0			ID4 (User Data-Word 5)
11	VBI_WORD_2[7:0]							0	0			ID5 (User Data-Word 6)
12	VBI_WORD_3[7:0]							0	0			ID6 (User Data-Word 7)
13	VBI_WORD_4[7:0]							0	0			ID7 (User Data-Word 8)
14	VBI_WORD_5[7:0]							0	0			ID8 (User Data-Word 9)
											Pad 0x200; these padding words may be present, depending on ancillary data type; user data-word	
n - 3	1	0	0	0	0	0	0	0	0	0		
n - 2	1	0	0	0	0	0	0	0	0	0		
n - 1	B8	Checksum							0	0		CS (checksum word)

<sup>1</sup> This mode does not fully comply with ITU-R BT.1364.

**Structure of VBI Words in the Ancillary Data Stream**

Each VBI data standard has been split into a clock-run-in (CRI), a framing code (FC), and a number of data bytes (n). The data packet in the ancillary stream includes only the FC and data bytes. Table 81 shows the format of VBI\_WORD\_x in the ancillary data stream.

Table 81. Structure of VBI Data-Words in the Ancillary Stream

Ancillary Data Byte No.	Byte Type	Description
VBI_WORD_1	FC0	Framing Code[23:16]
VBI_WORD_2	FC1	Framing Code[15:8]
VBI_WORD_3	FC2	Framing Code[7:0]
VBI_WORD_4	DB1	First data byte
...	...	...
VBI_WORD_N + 3	DBn	Last (n <sup>th</sup> ) data byte

**VDP Framing Code**

The length of the actual framing code depends on the VBI data standard. For uniformity, the length of the framing code reported in the ancillary data stream is always 24 bits. For standards with a smaller framing code length, the extra LSB bits are set to 0. The valid length of the framing code can be decoded from the VBI\_DATA\_STD bits available in ID0 (UDW 1). The framing code is always reported in the inverse-transmission order.

Table 82 shows the framing code and its valid length for VBI data standards supported by VDP.

**Example**

For teletext (B-WST), the framing code byte is 11100100 (0xE4), with bits shown in the order of transmission. VBI\_WORD\_1 = 0x27, VBI\_WORD\_2 = 0x00, and VBI\_WORD\_3 = 0x00 translated into UDWs in the ancillary data stream for nibble mode are as follows:

- UDW5[5:2] = 0010
- UDW6[5:2] = 0111
- UDW7[5:2] = 0000 (undefined bits set to 0)
- UDW8[5:2] = 0000 (undefined bits set to 0)
- UDW9[5:2] = 0000 (undefined bits set to 0)
- UDW10[5:2] = 0000 (undefined bits set to 0)

For byte mode,

- UDW5[9:2] = 0010\_0111
- UDW6[9:2] = 0000\_0000 (undefined bits set to 0)
- UDW7[9:2] = 0000\_0000 (undefined bits set to 0)

**Data Bytes**

VBI\_WORD\_4 to VBI\_WORD\_N + 3 contain the data-words that were decoded by the VDP in the transmission order. The position of bits in bytes is in the inverse transmission order.

For example, closed captioning has two user data bytes, as shown in Table 87.

The data bytes in the ancillary data stream are as follows:

VBI\_WORD\_4 = Byte 1[7:0]

VBI\_WORD\_5 = Byte 2[7:0]

The number of VBI\_WORDS for each VBI data standard and the total number of UDWs in the ancillary data stream is shown in Table 83.

**Table 82. Framing Code Sequence for Different VBI Standards**

VBI Standard	Length in Bits	Error-Free Framing Code Bits (in Order of Transmission)	Error-Free Framing Code Reported by VDP (in Reverse Order of Transmission)
TTXT_SYSTEM_A (PAL)	8	11100111	11100111
TTXT_SYSTEM_B (PAL)	8	11100100	00100111
TTXT_SYSTEM_B (NTSC)	8	11100100	00100111
TTXT_SYSTEM_C (PAL and NTSC)	8	11100111	11100111
TTXT_SYSTEM_D (PAL and NTSC)	8	11100101	10100111
WSS (PAL)	24	000111100011110000011111	111110000011110001111000
CCAP (NTSC and PAL)	3	001	100
CGMS (NTSC)	1	0	0

**Table 83. Total User Data-Words for Different VBI Standards<sup>1</sup>**

VBI Standard	ADF Mode	Framing Code UDWs	VBI Data-Words	No. of Padding Words	Total UDWs
TTXT_SYSTEM_A (PAL)	00 (nibble mode)	6	74	0	84
	01, 10 (byte mode)	3	37	0	44
TTXT_SYSTEM_B (PAL)	00 (nibble mode)	6	84	2	96
	01, 10 (byte mode)	3	42	3	52
TTXT_SYSTEM_B (NTSC)	00 (nibble mode)	6	68	2	80
	01, 10 (byte mode)	3	34	3	44
TTXT_SYSTEM_C (PAL and NTSC)	00 (nibble mode)	6	66	0	76
	01, 10 (byte mode)	3	33	2	42
TTXT_SYSTEM_D (PAL and NTSC)	00 (nibble mode)	6	68	2	80
	01, 10 (byte mode)	3	34	3	44
WSS (PAL)	00 (nibble mode)	6	4	2	16
	01, 10 (byte mode)	3	2	3	12
CCAP (NTSC and PAL)	00 (nibble mode)	6	4	2	16
	01, 10 (byte mode)	3	2	3	12
CGMS (NTSC)	00 (nibble mode)	6	6	0	16
	01, 10 (byte mode)	3	3 + 3	2	12

<sup>1</sup> The first four UDWs are always the ID.

### I<sup>2</sup>C Interface

Dedicated I<sup>2</sup>C readback registers are available for CCAP, CGMS, and WSS. Because teletext is a high data rate standard, data extraction is supported only through the ancillary data packet.

#### User Interface for I<sup>2</sup>C Readback Registers

The VDP decodes all enabled VBI data standards in real-time. Because the I<sup>2</sup>C access speed is much lower than the decoded rate, when the registers are accessed, they may be updated with data from the next line. To avoid this, VDP has a self-clearing clear bit and an available (AVL) status bit accompanying all I<sup>2</sup>C readback registers.

The user must clear the I<sup>2</sup>C readback register by writing a high to the clear bit. This resets the state of the available bit to low and indicates that the data in the associated readback registers is not valid. After the VDP decodes the next line of the corresponding VBI data, the decoded data is placed into the I<sup>2</sup>C readback register, and the available bit is set to high to indicate that valid data is now available.

Though the VDP decodes this VBI data in subsequent lines, if present, the decoded data is not updated to the readback registers until the clear bit is set high again. However, this data is available through the 656 ancillary data packets.

The clear and available bits are in the VDP\_STATUS\_CLEAR (0x78, Interrupt/VDP Map, write only) and VDP\_STATUS (0x78, Interrupt/VDP Map, read only) registers, respectively.

#### VDP—Content-Based Data Update

For certain standards such as WSS and CGMS, the information content in the signal transmitted remains the same over numerous lines, and the user may want to be notified only when there is a change in the information content or loss of the information content. The user must enable content-based updating for the required standard through the WSS\_CGMS\_CB\_CHANGE bit. This bit shows the availability of WSS and CGMS information only when its content has changed.

Content-based updating also applies to lines with lost data. Therefore, for standards like CGMS and WSS, if no data arrives in the next four lines programmed, the corresponding available bit in the VDP\_STATUS register is set high, and the content in the I<sup>2</sup>C registers for that standard is set to 0. The user must write high to the corresponding clear bit so that when a valid line is decoded after some time, the decoded results are available in the I<sup>2</sup>C registers, with the available status bit set high.

If content-based updating is enabled, the available bit is set high (assuming the clear bit was written) in the following cases:

- The data contents have changed.
- Data was being decoded and four lines with no data have been detected.
- No data was being decoded, and new data is now being decoded.

#### WSS\_CGMS\_CB\_CHANGE, Enable Content-Based Updating for WSS/CGMS, Address 0x9C[4], Interrupt/VDP Map

Setting WSS\_CGMS\_CB\_CHANGE to 0 disables content-based updating.

Setting WSS\_CGMS\_CB\_CHANGE to 1 (default) enables content-based updating.

#### VDP—Interrupt-Based Reading of VDP I<sup>2</sup>C Registers

Some VDP status bits are also linked to the interrupt request controller so that the user does not have to poll the available status bit. The user can configure the video decoder to trigger an interrupt request on the INTRQ pin in response to the valid data available in the I<sup>2</sup>C registers. This function is available for the following data types: CGMS or WSS. The user can select either triggering an interrupt request each time sliced data is available or triggering an interrupt request only when the sliced data has changed. Selection is made via the WSS\_CGMS\_CB\_CHANGE bit.

The sequence for the interrupt-based reading of the VDP I<sup>2</sup>C data registers is as follows for the CCAP standard:

1. The user unmarks the CCAP interrupt mask bit (Register 0x50, Bit 0, Interrupt/VDP Map = 1). CCAP data occurs on the incoming video. VDP slices CCAP data and places it into the VDP readback registers.
2. The VDP CCAP available bit, VDP\_CCAPD\_Q, goes high, and the VDP module signals to the interrupt controller to stimulate an interrupt request (for CCAP in this case).
3. The user reads the interrupt status bits (Interrupt/VDP Map) and sees that new CCAP data is available (Register 0x4E, Bit 0, Interrupt/VDP Map = 1).
4. The user writes 1 to the CCAP interrupt clear bit (Register 0x4E, Bit 0, Interrupt/VDP Map = 1) in the interrupt I<sup>2</sup>C space (this is a self-clearing bit). This clears the interrupt on the INTRQ pin but does not have an effect in the VDP I<sup>2</sup>C area.
5. The user reads the CCAP data from the VDP I<sup>2</sup>C area.
6. The user writes to Bit CC\_CLEAR in the VDP\_STATUS\_CLEAR register, (Register 0x78, Bit 0, User Sub Map 2 = 1) to signify that the CCAP data has been read (therefore the VDP CCAP can be updated at the next occurrence of CCAP).
7. The user goes back to Step 2.

**Interrupt Mask Register Details**

The following bits set the interrupt mask on the signal from the VDP VBI data slicer.

**VDP\_CCAPD\_MSK, Address 0x50[0], Interrupt/VDP Map**

Setting  $\overline{\text{VDP\_CCAPD\_MSK}}$  to 0 (default) masks (disables) the interrupt on the VDP\_CCAPD\_Q signal.

Setting  $\overline{\text{VDP\_CCAPD\_MSK}}$  to 1 un masks (enables) the interrupt on the VDP\_CCAPD\_Q signal.

**VDP\_CGMS\_WSS\_CHNGD\_MSK, Address 0x50[2],****Interrupt/VDP Map**

Setting  $\overline{\text{VDP\_CGMS\_WSS\_CHNGD\_MSK}}$  to 0 (default) masks (disables) the interrupt on the VDP\_CGMS\_WSS\_CHNGD\_Q signal.

Setting  $\overline{\text{VDP\_CGMS\_WSS\_CHNGD\_MSK}}$  to 1 un masks (enables) the interrupt on the VDP\_CGMS\_WSS\_CHNGD\_Q signal.

**Interrupt Status Register Details**

The following read-only bits contain data detection information from the VDP module since the status bit was last cleared or unmasked.

**VDP\_CCAPD\_Q, Address 0x4E[0], Interrupt/VDP Map**

When VDP\_CCAPD\_Q is 0 (default), CCAP data has not been detected.

When VDP\_CCAPD\_Q is 1, CCAP data has been detected.

**VDP\_CGMS\_WSS\_CHNGD\_Q, Address 0x4E[2],****Interrupt/VDP Map**

When VDP\_CGMS\_WSS\_CHNGD\_Q is 0 (default), CGMS or WSS data has not been detected.

VDP\_CGMS\_WSS\_CHNGD\_Q is also 0 if the CGMS or WSS data state has not changed since last cleared (see Interrupt Status Clear Register Details).

When VDP\_CGMS\_WSS\_CHNGD\_Q is 1, CGM or WSS data has been detected.

**Interrupt Status Clear Register Details**

It is not necessary to write 0 to these write-only bits because they automatically reset after they have been set to 1 (self-clearing).

**VDP\_CCAPD\_CLR, Address 0x4F[0],****Interrupt/VDP Map**

Setting VDP\_CCAPD\_CLR to 1 clears the VDP\_CCAPD\_Q bit.

**VDP\_CGMS\_WSS\_CHNGD\_CLR, Address 0x4F[2],****Interrupt/VDP Map**

Setting VDP\_CGMS\_WSS\_CHNGD\_CLR to 1 clears the VDP\_CGMS\_WSS\_CHNGD\_Q bit.

**I<sup>2</sup>C READBACK REGISTERS****Teletext**

Because teletext is a high data rate standard, the decoded bytes are available only as ancillary data. However, a TTXT\_AVL bit has been provided in I<sup>2</sup>C so that the user can check whether the VDP has detected teletext. Note that the TTXT\_AVL bit is a plain status bit and does not use the protocol identified in the I<sup>2</sup>C Interface section.

**TTXT\_AVL, Teletext Detected Status, Address 0x78[7], Interrupt/VDP Map, Read Only**

When TTXT\_AVL is 0, teletext was not detected.

When TTXT\_AVL is 1, teletext was detected.

**WST Packet Decoding**

For WST only, the VDP decodes the magazine and row address of teletext packets and further decodes the packet's 8 × 4 hamming coded words. This feature can be disabled using the WST\_PKT\_DECODE\_DISABLE bit (Bit 3, Register 0x60, user sub map). This feature is valid for WST only.

**WST\_PKT\_DECODE\_DISABLE, Disable Hamming****Decoding of Bytes in WST, Address 0x60[3],****Interrupt/VDP Map**

Setting WST\_PKT\_DECODE\_DISABLE to 0 enables hamming decoding of WST packets.

Setting WST\_PKT\_DECODE\_DISABLE to 1 (default) disables hamming decoding of WST packets.

For hamming-coded bytes, the de-hammed nibbles are output along with some error information from the hamming decoder as follows:

- Input hamming coded byte: {D3, P3, D2, P2, D1, P1, D0, P0} (bits in decoded order)
- Output dehammed byte: {E1, E0, 0, 0, D3', D2', D1', D0'} (Di' – corrected bits, Ei error information).

**Table 84. Error Bits in the Dehammed Output Byte**

E[1:0]	Error Information	Output Data Bits in Nibble
00	No errors detected	Okay
01	Error in P4	Okay
10	Double error	Bad
11	Single error found and corrected	Okay

Table 85 describes the WST packets that are decoded.



Table 85. WST Packet Description

Packet	Byte	Description
Header Packet (X/00)	1st 2nd 3rd 4th 5th to 10th 11th to 42nd	Magazine number—Dehammed Byte 4 Row number—Dehammed Byte 5 Page number—Dehammed Byte 6 Page number—Dehammed Byte 7 Control bytes—Dehammed Byte 8 to Byte 13 Raw data bytes
Text Packets (X/01 to X/25)	1st 2nd 3rd to 42nd	Magazine number—Dehammed Byte 4 Row number—Dehammed Byte 5 Raw data bytes
8/30 (Format 1) Packet Design Code = 0000 or 0001 UTC	1st 2nd 3rd 4th to 10th 11th to 23rd 24th to 42nd	Magazine number—Dehammed Byte 4 Row number—Dehammed Byte 5 Design code—Dehammed Byte 6 De-hammed initial teletext page, Byte 7 to Byte 12 UTC bytes—Dehammed Byte 13 to Byte 25 Raw status bytes
8/30 (Format 2) Packet Design Code = 0010 or 0011 PDC	1st 2nd 3rd 4th to 10th 11th to 23rd 24th to 42nd	Magazine number—Dehammed Byte 4 Row number—Dehammed Byte 5 Design code—Dehammed Byte 6 Dehammed initial teletext page, Byte 7 to Byte 12 PDC bytes—Dehammed Byte 13 to Byte 25 Raw status bytes
X/26, X/27, X/28, X/29, X/30, X/31 <sup>1</sup>	1st 2nd 3rd 4th to 42nd	Magazine number—Dehammed Byte 4 Row number—Dehammed Byte 5 Design code—Dehammed Byte 6 Raw data bytes

<sup>1</sup> For X/26, X/28, and X/29, further decoding needs 24 × 18 hamming decoding. Not supported at present.

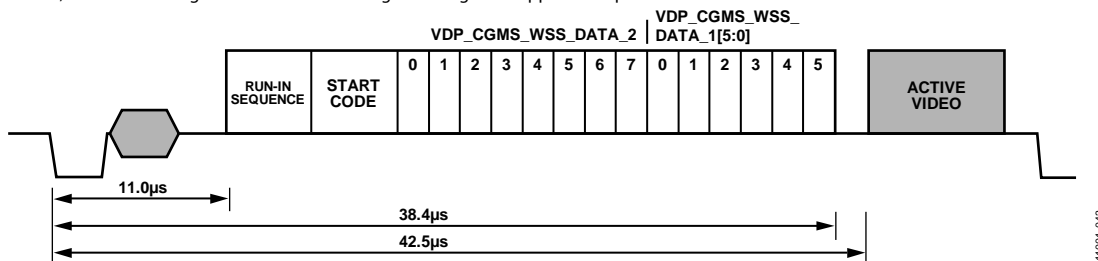


Figure 42. WSS Waveform

**CGMS and WSS**

The CGMS and WSS data packets convey the same type of information for different video standards. WSS is for PAL and CGMS is for NTSC; therefore, the CGMS and WSS readback registers are shared. WSS is biphase coded; the VDP performs a biphase decoding to produce the 14 raw WSS bits in the CGMS/WSS readback I<sup>2</sup>C registers and to set the CGMS\_WSS\_AVL bit.

**CGMS\_WSS\_CLEAR, CGMS/WSS Clear, Address 0x78[2], Interrupt/VDP Map, Write Only, Self-Clearing**

Setting CGMS\_WSS\_CLEAR to 0 does not reinitialize the CGMS/WSS readback registers.

Setting CGMS\_WSS\_CLEAR to 1 reinitializes the CGMS/WSS readback registers.

**CGMS\_WSS\_AVL, CGMS/WSS Available, Address 0x78[2], User Sub Map, Read Only**

When CGMS\_WSS\_AVL is 0, CGMS/WSS was not detected.

When CGMS\_WSS\_AVL is 1, CGMS/WSS was detected.

**VDP\_CGMS\_WSS\_DATA\_0[3:0], Address 0x7D[3:0];**

**VDP\_CGMS\_WSS\_DATA\_1[7:0], Address 0x7E[7:0];**

**VDP\_CGMS\_WSS\_DATA\_2[7:0], Address 0x7F[7:0];**

**Interrupt/VDP Map, Read Only**

These bits hold the decoded CGMS or WSS data.

Refer to Figure 42 and Figure 43 for the I<sup>2</sup>C-to-WSS and I<sup>2</sup>C-to-CGMS bit mapping.

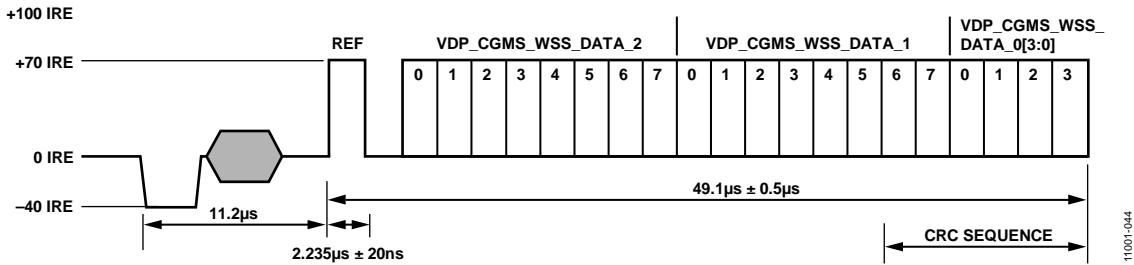


Figure 43. CGMS Waveform

Table 86. CGMS Readback Registers (These registers are readback registers; default value does not apply.)

Signal Name	Register Location	Dec	Hex
CGMS_WSS_DATA_0[3:0]	VDP_CGMS_WSS_DATA_0[3:0]	125	0x7D
CGMS_WSS_DATA_1[7:0]	VDP_CGMS_WSS_DATA_1[7:0]	126	0x7E
CGMS_WSS_DATA_2[7:0]	VDP_CGMS_WSS_DATA_2[7:0]	127	0x7F

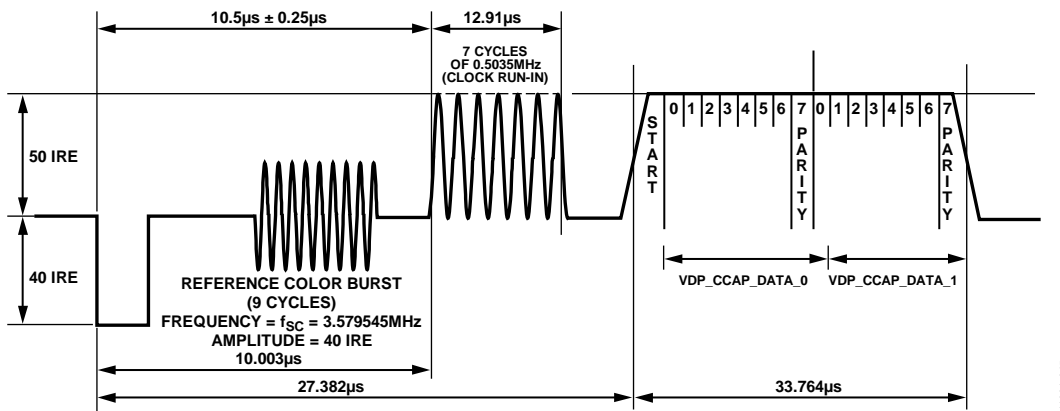


Figure 44. CCAP Waveform and Decoded Data Correlation

Table 87. CCAP Readback Registers (These registers are readback registers; default value does not apply.)

Signal Name	Register Location	Dec	Hex
CCAP_BYTE_1[7:0]	VDP_CCAP_DATA_0[7:0]	121	0x79
CCAP_BYTE_2[7:0]	VDP_CCAP_DATA_1[7:0]	122	0x7A

**CCAP**

Two bytes of decoded closed caption data are available in the I<sup>2</sup>C registers. The field information of the decoded CCAP data can be obtained from the CC\_EVEN\_FIELD bit (Register 0x78).

**CC\_CLEAR, Closed Caption Clear, Address 0x78[0], Interrupt/VDP Map, Write Only, Self-Clearing**

Setting CC\_CLEAR to 0 does not reinitializes the CCAP readback registers.

Setting CC\_CLEAR to 1 reinitializes the CCAP readback registers.

**CC\_AVL, Closed Caption Available, Address 0x78[0], Interrupt/VDP Map, Read Only**

When CC\_AVL is 0, closed captioning is not detected.

When CC\_AVL is 1, closed captioning is detected.

**CC\_EVEN\_FIELD, Address 0x78[1], Interrupt/VDP Map, Read Only**

Identifies the field from which the CCAP data was decoded.

When CC\_EVEN\_FIELD is 0, closed captioning was detected from an odd field.

When CC\_EVEN\_FIELD is 1, closed captioning was detected from an even field.

**VDP\_CCAP\_DATA\_0, Address 0x79[7:0], Interrupt/VDP Map, Read Only**

Decoded Byte 1 of CCAP data.

**VDP\_CCAP\_DATA\_1, Address 0x7A[7:0], Interrupt/VDP Map, Read Only**

Decoded Byte 2 of CCAP data.

### Letterbox Detection

Incoming video signals may conform to different aspect ratios (16:9 wide screen or 4:3 standard). For certain transmissions in the wide-screen format, a digital sequence (WSS) is transmitted with the video signal. If a WSS sequence is provided, the aspect ratio of the video can be derived from the digitally decoded bits that WSS contains.

In the absence of a WSS sequence, letterbox detection can be used to find wide-screen signals. The detection algorithm examines the active video content of lines at the start and end of a field. If black lines are detected, this may indicate that the currently shown picture is in wide-screen format.

The active video content (luminance magnitude) over a line of video is summed together. At the end of a line, this accumulated value is compared with a threshold, and a decision is made as to whether or not a particular line is black. The threshold value needed may depend on the type of input signal; some control is provided via LB\_TH[4:0].

#### Detection at the Start of a Field

The ADV7182 expects a section of at least six consecutive black lines of video at the top of a field. After those lines are detected, LB\_LCT[7:0] reports the number of black lines that were actually found. By default, the ADV7182 starts looking for those black lines in sync with the beginning of active video, for example, immediately after the last VBI video line. LB\_SL[3:0] allows the user to set the start of letterbox detection from the beginning of a frame on a line-by-line basis. The detection window closes in the middle of the field.

#### Detection at the End of a Field

The ADV7182 expects at least six continuous lines of black video at the bottom of a field before reporting the number of lines actually found via the LB\_LCB[7:0] value. The activity window for letterbox detection (end of field) starts in the middle of an active field. Its end is programmable via LB\_EL[3:0].

#### Detection at the Midrange

Some transmissions of wide-screen video include subtitles within the lower black box. If the ADV7182 finds at least two black lines followed by some more nonblack video, for example, the subtitle followed by the remainder of the bottom black block, it reports a midcount via LB\_LCM[7:0]. If no subtitles are found, LB\_LCM[7:0] reports the same number as LB\_LCB[7:0].

There is a two-field delay in reporting any line count parameter.

There is no letterbox detected bit. Read the LB\_LCT[7:0] and LB\_LCB[7:0] register values to determine whether the letterbox-type video is present in the software.

LB\_LCT[7:0], Letterbox Line Count Top, Address 0x9B[7:0];  
LB\_LCM[7:0], Letterbox Line Count Mid, Address 0x9C[7:0];  
LB\_LCB[7:0], Letterbox Line Count Bottom, Address 0x9D[7:0]

Table 88. LB\_LCx Access Information

Signal Name	Address
LB_LCT[7:0]	0x9B
LB_LCM[7:0]	0x9C
LB_LCB[7:0]	0x9D

LB\_TH[4:0], Letterbox Threshold Control, Address 0xDC[4:0]

Table 89. LB\_TH Function

LB_TH[4:0]	Description
01100 (default)	Default threshold for detection of black lines
01101 to 10000	Increase threshold (need larger active video content before identifying nonblack lines)
00000 to 01011	Decrease threshold (even small noise levels can cause the detection of nonblack lines)

LB\_SL[3:0], Letterbox Start Line, Address 0xDD[7:4]

The LB\_SL[3:0] bits are set at 1100 by default. For an NTSC signal, this window is from Line 31 to Line 294.

By changing the bits to 0100, the detection window starts on Line 23 and ends on Line 286.

LB\_EL[3:0], Letterbox End Line, Address 0xDD[3:0]

The LB\_EL[3:0] bits are set at 1100 by default. This means that the letterbox window ends with the last active video line. For an NTSC signal, this window is from Line 261 to Line 524.

By changing the bits to 1101, the detection window starts on Line 262 and ends on Line 255.

## PIXEL PORT CONFIGURATION

The [ADV7182](#) has a very flexible pixel port that can be configured in a variety of formats to accommodate downstream ICs. The ordering of components, for example, Cr vs. Cb can be changed. See the SWPC, Swap Pixel Cr/Cb, Address 0x27[7] section.

### SWPC, Swap Pixel Cr/Cb, Address 0x27[7]

This bit allows Cr and Cb samples to be swapped.

When SWPC is 0 (default), no swapping is allowed. When SWPC is 1, the Cr and Cb values can be swapped.

### LLC\_PAD\_SEL[2:0] LLC Output Selection, Address 0x8F[6:4]

The following I<sup>2</sup>C write allows the user to select between LLC (nominally at 27 MHz) and LLC (nominally at 13.5 MHz).

The LLC signal is useful for LLC-compatible wide bus (16-bit) output modes. The LLC signal and data on the data bus are synchronized. By default, the rising edge of LLC/LLC is aligned with the Y data; the falling edge occurs when the data bus holds C data. The polarity of the clock, and therefore the Y/C assignments to the clock edges, can be altered by using the polarity LLC pin.

When LLC\_PAD\_SEL is 000, the output is nominally 27 MHz LLC on the LLC pin (default).

When LLC\_PAD\_SEL is 101, the output is nominally 13.5 MHz LLC on the LLC pin.

## MPU PORT DESCRIPTION

The **ADV7182** supports a 2-wire (I<sup>2</sup>C-compatible) serial interface. Two inputs, serial data (SDATA) and serial clock (SCLK), carry information between the **ADV7182** and the system I<sup>2</sup>C master controller. Each slave device is recognized by a unique address. The **ADV7182** I<sup>2</sup>C port allows the user to set up and configure the decoder and to read back the captured VBI data. The **ADV7182** has four possible slave addresses for both read and write operations, depending on the logic level of the ALSB pin. The four unique addresses are shown in Table 90. The **ADV7182** ALSB pin controls Bit 1 of the slave address. By altering the ALSB, it is possible to control two **ADV7182s** in an application without the conflict of using the same slave address. The LSB (Bit 0) sets either a read or write operation. Logic 1 corresponds to a read operation, and Logic 0 corresponds to a write operation.

**Table 90. I<sup>2</sup>C Address for ADV7182**

ALSB	R/W	Slave Address
0	0	0x40
0	1	0x41
1	0	0x42
1	1	0x43

To control the device on the bus, a specific protocol must be followed. First, the master initiates a data transfer by establishing a start condition, which is defined by a high-to-low transition on SDATA while SCLK remains high. This indicates that an address/data stream follows. All peripherals respond to the start condition and shift the next eight bits (the 7-bit address plus the R/W bit). The bits are transferred from MSB down to LSB. The peripheral that recognizes the transmitted address responds by pulling the data line low during the ninth clock pulse; this is known as an acknowledge bit. All other devices withdraw from the bus at this point and maintain an idle condition. The idle condition is where the device monitors the SDATA and SCLK lines for the start condition and the correct transmitted address. The R/W

bit determines the direction of the data. Logic 0 on the LSB of the first byte means that the master writes information to the peripheral. Logic 1 on the LSB of the first byte means that the master reads information from the peripheral.

The **ADV7182** acts as a standard slave device on the bus. The data on the SDATA pin is eight bits long, supporting the 7-bit address plus the R/W bit. The device has subaddresses to enable access to the internal registers. It, therefore, interprets the first byte as the device address and the second byte as the starting subaddress. The subaddresses auto-increment, allowing data to be written to or read from the starting subaddress. A data transfer is always terminated by a stop condition. The user can also access any unique subaddress register on a one-by-one basis without updating all the registers.

Stop and start conditions can be detected at any stage during the data transfer. If these conditions are asserted out of sequence with normal read and write operations, they cause an immediate jump to the idle condition. During a given SCLK high period, only issue one start condition, one stop condition, or a single stop condition followed by a single start condition. If an invalid subaddress is issued, the **ADV7182** does not issue an acknowledge and returns to the idle condition.

In autoincrement mode, if the user exceeds the highest subaddress, the following action is taken:

- In read mode, the highest subaddress register contents continue to be output until the master device issues a no acknowledge. This indicates the end of a read. A no acknowledge condition occurs when the SDATA line is not pulled low on the ninth pulse.
- In write mode, the data for the invalid byte is not loaded into any subaddress register. A no acknowledge is issued by the **ADV7182**, and the part returns to the idle condition.

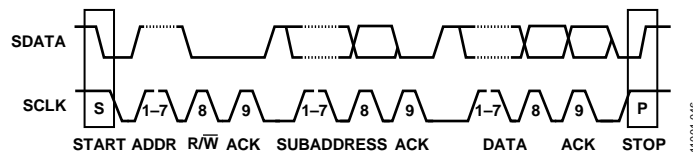


Figure 45. Bus Data Transfer

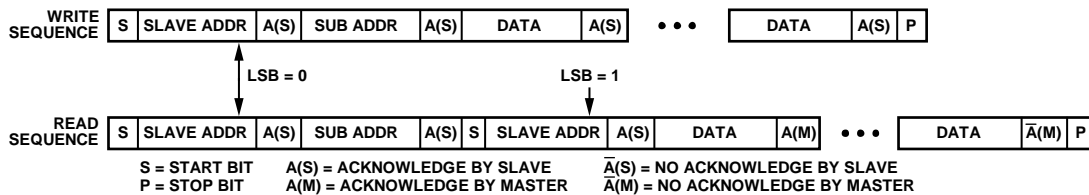


Figure 46. Read and Write Sequence

**REGISTER ACCESS**

The MPU can write to or read from all of the ADV7182 registers except the subaddress register, which is write only. The subaddress register determines which register the next read or write operation accesses. All communications with the part through the bus start with an access to the subaddress register. A read/write operation is then performed from or to the target address, which increments to the next address until a stop command on the bus is performed. Note that only the registers listed in the I2C Register Maps section are supported.

**REGISTER PROGRAMMING**

The following sections describe the configuration for each register. The communication register is an 8-bit, write-only register. After the part is accessed over the bus and a read/write operation is selected, the subaddress is set up. The subaddress register determines to or from which register the operation takes place.

**SUB\_USR\_EN, Address 0x0E[6:5]**

The ADV7182 has three I<sup>2</sup>C maps. The main register map (see Table 91) is the map that is available by default. The other two maps are accessed using the SUB\_USR\_EN bit (Address 0x0E). When programming of these maps is completed, it is necessary to write to the SUB\_USR\_EN bit to return to the main register map (see Table 91).

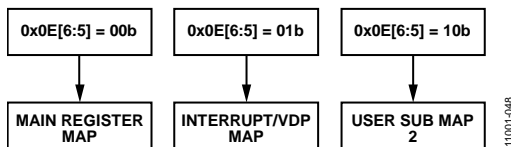


Figure 47. Register Access—Main Register Map, Interrupt/VDP Map, and User Sub Map 2

**Register Select (SR7 to SR0)**

These bits are set up to point to the required starting address.

**I<sup>2</sup>C SEQUENCER**

An I<sup>2</sup>C sequencer is used when a parameter exceeds eight bits and is, therefore, distributed over two or more I<sup>2</sup>C registers, for example, HSB[10:0].

When such a parameter is changed using two or more I<sup>2</sup>C write operations, the parameter can hold an invalid value for the time between the first I<sup>2</sup>C being completed and the last I<sup>2</sup>C being completed. In other words, the top bits of the parameter may hold the new value while the remaining bits of the parameter still hold the previous value.

To avoid this problem, the I<sup>2</sup>C sequencer holds the updated bits of the parameter in local memory, and all bits of the parameter are updated together once the last register write operation has completed.

The correct operation of the I<sup>2</sup>C sequencer relies on the following:

- All I<sup>2</sup>C registers for the parameter in question must be written to in order of ascending addresses. For example, for HSB[10:0], write to Address 0x34 first, followed by 0x35, and so on.
- No other I<sup>2</sup>C can take place between the two (or more) I<sup>2</sup>C writes for the sequence. For example, for HSB[10:0], write to Address 0x34 first, immediately followed by 0x35, and so on.

# I<sup>2</sup>C REGISTER MAPS

To access all the registers listed in Table 91, SUB\_USR\_EN in Register Address 0x0E must be programmed to 00b. All read only registers are left blank.

**Table 91. Main Register Map Details**

Address		Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	(Hex)
Dec	Hex												
0	00	Input control	RW				INSEL[4]	INSEL[3]	INSEL[2]	INSEL[1]	INSEL[0]	00001110	0E
1	01	Video Selection 1	RW		ENHSPLL	BETACAM		ENVSPROC				11001000	C8
2	02	Video Selection 2	RW	VID_SEL[3]	VID_SEL[2]	VID_SEL[1]	VID_SEL[0]					00000100	04
3	03	Output control	RW	VBI_EN	TOD							01001100	4C
4	04	Extended output control	RW	BT.656-4				TIM_OE	BL_C_VBI	EN_SFL_PIN	Range	00110101	35
5	05	Reserved											
6	06	Reserved											
7	07	Autodetect enable	RW	AD_SEC525_EN	AD_SECAM_EN	AD_N443_EN	AD_P60_EN	AD_PALN_EN	AD_PALM_EN	AD_NTSC_EN	AD_PAL_EN	01111111	7F
8	08	Contrast	RW	CON[7]	CON[6]	CON[5]	CON[4]	CON[3]	CON[2]	CON[1]	CON[0]	10000000	80
9	09	Reserved											
10	0A	Brightness Adjust	RW	BRI[7]	BRI[6]	BRI[5]	BRI[4]	BRI[3]	BRI[2]	BRI[1]	BRI[0]	00000000	00
11	0B	Hue Adjust	RW	HUE[7]	HUE[6]	HUE[5]	HUE[4]	HUE[3]	HUE[2]	HUE[1]	HUE[0]	00000000	00
12	0C	Default Value Y	RW	DEF_Y[5]	DEF_Y[4]	DEF_Y[3]	DEF_Y[2]	DEF_Y[1]	DEF_Y[0]	DEF_VAL_AUTO_EN	DEF_VAL_EN	00110110	36
13	0D	Default Value C	RW	DEF_C[7]	DEF_C[6]	DEF_C[5]	DEF_C[4]	DEF_C[3]	DEF_C[2]	DEF_C[1]	DEF_C[0]	01111100	7C
14	0E	ADI Control 1	RW		SUB_USR_EN[1]	SUB_USR_EN[0]						00000000	00
15	0F	Power management	RW	Reset		PWRDWN						00100000	20
16	10	Status 1	R	COL_KILL	AD_RESULT[2]	AD_RESULT[1]	AD_RESULT[0]	FOLLOW_PW	FSC_LOCK	LOST_LOCK	IN_LOCK		
17	11	IDENT	R	IDENT[7]	IDENT[6]	IDENT[5]	IDENT[4]	IDENT[3]	IDENT[2]	IDENT[1]	IDENT[0]	00011100	1C
18	12	Status 2	R			FSC_NSTD	LL_NSTD	MV_AGC_DET	MV_PS_DET	MVCS_T3	MVCS_DET		
19	13	Status 3	R	PAL_SW_LOCK	Interlaced	STD_FLD_LEN	FREE_RUN_ACT	Reserved	SD_OP_50Hz	Reserved	INST_HLOCK		
20	14	Analog clamp control	RW				CCLN		FREE_RUN_PAT_SEL2	FREE_RUN_PAT_SEL1	FREE_RUN_PAT_SEL0	00010000	10
21	15	Digital Clamp Control 1	RW		DCT[1]	DCT[0]	DCFE					0000xxxx	00
22	16	Reserved											
23	17	Shaping Filter Control 1	RW	CSFM[2]	CSFM[1]	CSFM[0]	YSFM[4]	YSFM[3]	YSFM[2]	YSFM[1]	YSFM[0]	00000001	01
24	18	Shaping Filter Control 2	RW	WYSFMOVR			WYSFM[4]	WYSFM[3]	WYSFM[2]	WYSFM[1]	WYSFM[0]	10010011	93
25	19	Comb filter control	RW					NSFSEL[1]	NSFSEL[0]	PSFSEL[1]	PSFSEL[0]	11110001	F1
29	1D	ADI Control 2	RW	TRI_LLC								11000xxx	C0
39	27	Pixel delay control	RW	SWPC	AUTO_PDC_EN	CTA[2]	CTA[1]	CTA[0]		LTA[1]	LTA[0]	01011000	58
43	2B	Misc gain control	RW		CKE						PW_UPD	11100001	E1
44	2C	AGC mode control	RW		LACG[2]	LAGC[1]	LAGC[0]			CAGC[1]	CAGC[0]	10101110	AE
45	2D	Chroma Gain Control 1	W	CAGT[1]	CAGT[0]			CMG[11]	CMG[10]	CMG[9]	CMG[8]	11110100	F4
45	2D	Chroma Gain 1	R					CG[11]	CG[10]	CG[9]	CG[8]		
46	2E	Chroma Gain Control 2	W	CMG[7]	CMG[6]	CMG[5]	CMG[4]	CMG[3]	CMG[2]	CMG[1]	CMG[0]	00000000	00
46	2E	Chroma Gain 2	R	CG[7]	CG[6]	CG[5]	CG[4]	CG[3]	CG[2]	CG[1]	CG[0]		
47	2F	Luma Gain Control 1	W	LAGT[1]	LAGT[0]			LMG[11]	LMG[10]	LMG[9]	LMG[8]	1111xxxx	F0
47	2F	Luma Gain 1	R					LG[11]	LG[10]	LG[9]	LG[8]		
48	30	Luma Gain Control 2	W	LMG[7]	LMG[6]	LMG[5]	LMG[4]	LMG[3]	LMG[2]	LMG[1]	LMG[0]	xxxxxxx	00
48	30	Luma Gain 2	R	LG[7]	LG[6]	LG[5]	LG[4]	LG[3]	LG[2]	LG[1]	LG[0]		
49	31	VS/FIELD Control 1	RW				NEWAVMODE	HVSTIM				00000010	02
50	32	VS/FIELD Control 2	RW	VSBHO	VSBHE							01000001	41
51	33	VS/FIELD Control 3	RW	VSEHO	VSEHE							10000100	84
52	34	HS Position Control 1	RW		HSB[10]	HSB[9]	HSB[8]		HSE[10]	HSE[9]	HSE[8]	00000000	00
53	35	HS Position Control 2	RW	HSB[7]	HSB[6]	HSB[5]	HSB[4]	HSB[3]	HSB[2]	HSB[1]	HSB[0]	00000010	02
54	36	HS Position Control 3	RW	HSE[7]	HSE[6]	HSE[5]	HSE[4]	HSE[3]	HSE[2]	HSE[1]	HSE[0]	00000000	00
55	37	Polarity	RW	PHS		PVS		PF			PCLK	00010001	09
56	38	NTSC comb control	RW	CTAPSN[1]	CTAPSN[0]	CCMN[2]	CCMN[1]	CCMN[0]	YCMN[2]	YCMN[1]	YCMN[0]	10000000	80
57	39	PAL comb control	RW	CTAPSP[1]	CTAPSP[0]	CCMP[2]	CCMP[1]	CCMP[0]	YCMP[2]	YCMP[1]	YCMP[0]	11000000	C0
58	3A	ADC control	RW					PWRDWN_MUX_0	PWRDWN_MUX_1	PWRDWN_MUX_2	MUX_PDN override	00000000	00
61	3D	Manual window control	RW		CKILLTHR[2]	CKILLTHR[1]	CKILLTHR[0]					00100010	22
65	41	Resample control	RW		SFL_INV							00000001	01
77	4D	CTI DNR Control 1	RW			DNR_EN		CTI_AB[1]	CTI_AB[0]	CTI_AB_EN	CTI_EN	11101111	EF
78	4E	CTI DNR Control 2	RW	CTI_C_TH[7]	CTI_C_TH[6]	CTI_C_TH[5]	CTI_C_TH[4]	CTI_C_TH[3]	CTI_C_TH[2]	CTI_C_TH[1]	CTI_C_TH[0]	00001000	08
80	50	DNR Noise Threshold 1	RW	DNR_TH[7]	DNR_TH[6]	DNR_TH[5]	DNR_TH[4]	DNR_TH[3]	DNR_TH[2]	DNR_TH[1]	DNR_TH[0]	00001000	08
81	51	Lock count	RW	FSCLE	SRLS	COL[2]	COL[1]	COL[0]	CIL[2]	CIL[1]	CIL[0]	00100100	24
96	60	ADC Switch 3	RW						MUX3[2]	MUX3[1]	MUX3[0]	00010000	10
106	6A	Output Sync Select 1	RW						HS_OUT_SEL[2]	HS_OUT_SEL[1]	HS_OUT_SEL[0]	00000000	00
107	6B	Output Sync Select 2	RW		FLD_OUT_SEL[2]	FLD_OUT_SEL[1]	FLD_OUT_SEL[0]					00010010	12
143	8F	Free-Run Line Length 1	W		LLC_PAD_SEL[2]	LLC_PAD_SEL[1]	LLC_PAD_SEL[0]					00000000	00
153	99	CCAP1	R	CCAP1[7]	CCAP1[6]	CCAP1[5]	CCAP1[4]	CCAP1[3]	CCAP1[2]	CCAP1[1]	CCAP1[0]		

Address		Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	(Hex)
Dec	Hex												
154	9A	CCAP2	R	CCAP2[7]	CCAP2[6]	CCAP2[5]	CCAP2[4]	CCAP2[3]	CCAP2[2]	CCAP2[1]	CCAP2[0]		
155	9B	Letterbox 1	R	LB_LCT[7]	LB_LCT[6]	LB_LCT[5]	LB_LCT[4]	LB_LCT[3]	LB_LCT[2]	LB_LCT[1]	LB_LCT[0]		
156	9C	Letterbox 2	R	LB_LCM[7]	LB_LCM[6]	LB_LCM[5]	LB_LCM[4]	LB_LCM[3]	LB_LCM[2]	LB_LCM[1]	LB_LCM[0]		
157	9D	Letterbox 3	R	LB_LCB[7]	LB_LCB[6]	LB_LCB[5]	LB_LCB[4]	LB_LCB[3]	LB_LCB[2]	LB_LCB[1]	LB_LCB[0]		
178	B2	CRC enable	W						CRC_ENABLE			00011100	1C
195	C3	ADC Switch 1	RW	Reserved	MUX1[2]	MUX1[1]	MUX1[0]	Reserved	MUX0[2]	MUX0[1]	MUX0[0]	xxxxxxx	00
196	C4	ADC Switch 2	RW	MAN_MUX_EN				Reserved	MUX2[2]	MUX2[1]	MUX2[0]	0xxxxxxx	00
220	DC	Letterbox Control 1	RW				LB_TH[4]	LB_TH[3]	LB_TH[2]	LB_TH[1]	LB_TH[0]	10101100	AC
221	DD	Letterbox Control 2	RW	LB_SL[3]	LB_SL[2]	LB_SL[1]	LB_SL[0]	LB_EL[3]	LB_EL[2]	LB_EL[1]	LB_EL[0]	01001100	4C
222	DE	ST Noise Readback 1	R					ST_NOISE_VLD	ST_NOISE[10]	ST_NOISE[9]	ST_NOISE[8]		
223	DF	ST Noise Readback 2	R	ST_NOISE[7]	ST_NOISE[6]	ST_NOISE[5]	ST_NOISE[4]	ST_NOISE[3]	ST_NOISE[2]	ST_NOISE[1]	ST_NOISE[0]		
225	E1	SD offset Cb channel	RW	SD_OFF_Cb[7]	SD_OFF_Cb[6]	SD_OFF_Cb[5]	SD_OFF_Cb[4]	SD_OFF_Cb[3]	SD_OFF_Cb[2]	SD_OFF_Cb[1]	SD_OFF_Cb[0]	10000000	80
226	E2	SD offset Cr channel	RW	SD_OFF_Cr[7]	SD_OFF_Cr[6]	SD_OFF_Cr[5]	SD_OFF_Cr[4]	SD_OFF_Cr[3]	SD_OFF_Cr[2]	SD_OFF_Cr[1]	SD_OFF_Cr[0]	10000000	80
227	E3	SD saturation Cb channel	RW	SD_SAT_Cb[7]	SD_SAT_Cb[6]	SD_SAT_Cb[5]	SD_SAT_Cb[4]	SD_SAT_Cb[3]	SD_SAT_Cb[2]	SD_SAT_Cb[1]	SD_SAT_Cb[0]	10000000	80
228	E4	SD saturation Cr channel	RW	SD_SAT_Cr[7]	SD_SAT_Cr[6]	SD_SAT_Cr[5]	SD_SAT_Cr[4]	SD_SAT_Cr[3]	SD_SAT_Cr[2]	SD_SAT_Cr[1]	SD_SAT_Cr[0]	10000000	80
229	E5	NTSC V bit begin	RW	NVBEGDELO	NVBEGDELE	NVBEGSIGN	NVBEG[4]	NVBEG[3]	NVBEG[2]	NVBEG[1]	NVBEG[0]	00100101	25
230	E6	NTSC V bit end	RW	NVNDDELO	NVNDDELE	NVNDSIGN	NVND[4]	NVND[3]	NVND[2]	NVND[1]	NVND[0]	00001000	04
231	E7	NTSC F bit toggle	RW	NFTOGDELO	NFTOGDELE	NFTOGSIGN	NFTOG[4]	NFTOG[3]	NFTOG[2]	NFTOG[1]	NFTOG[0]	01100011	63
232	E8	PAL V bit begin	RW	PVBEGDELO	PVBEGDELE	PVBEGSIGN	PVBEG[4]	PVBEG[3]	PVBEG[2]	PVBEG[1]	PVBEG[0]	01100101	65
233	E9	PAL V bit end	RW	PVNDDELO	PVNDDELE	PVNDSIGN	PVND[4]	PVND[3]	PVND[2]	PVND[1]	PVND[0]	00010100	14
234	EA	PAL F bit toggle	RW	PFTOGDELO	PFTOGDELE	PFTOGSIGN	PFTOG[4]	PFTOG[3]	PFTOG[2]	PFTOG[1]	PFTOG[0]	01100011	63
235	EB	Vblank Control 1	RW	NVBIOLCM[1]	NVBIOLCM[0]	NVBIELCM[1]	NVBIELCM[0]	PVBIOLCM[1]	PVBIOLCM[0]	PVBIELCM[1]	PVBIELCM[0]	01010101	55
236	EC	Vblank Control 2	RW	NVBIOCCM[1]	NVBIOCCM[0]	NVBIECM[1]	NVBIECM[0]	PVBIOCCM[1]	PVBIOCCM[0]	PVBIECM[1]	PVBIECM[0]	01010101	55
243	F3	AFE_CONTROL 1	RW				AA_FILT_MAN_OVR	AA_FILT_EN[3]	AA_FILT_EN[2]	AA_FILT_EN[1]	AA_FILT_EN[0]	00000000	00
244	F4	Drive strength	RW	GLITCH_FILT_BYF		DR_STR[1]	DR_STR[0]	DR_STR_C[1]	DR_STR_C[0]	DR_STR_S[1]	DR_STR_S[0]	0x010101	15
248	F8	IF comp control	RW						IFFILTSEL[2]	IFFILTSEL[1]	IFFILTSEL[0]	00000000	00
249	F9	VS mode control	RW					VS_COAST_MODE[1]	VS_COAST_MODE[0]	EXTEND_VS_MIN_FREQ	EXTEND_VS_MAX_FREQ	00000011	03
251	FB	Peaking gain	RW	PEAKING_GAIN[7]	PEAKING_GAIN[6]	PEAKING_GAIN[5]	PEAKING_GAIN[4]	PEAKING_GAIN[3]	PEAKING_GAIN[2]	PEAKING_GAIN[1]	PEAKING_GAIN[0]	01000000	40
252	FC	DNR Noise Threshold 2	RW	DNR_TH2[7]	DNR_TH2[6]	DNR_TH2[5]	DNR_TH2[4]	DNR_TH2[3]	DNR_TH2[2]	DNR_TH2[1]	DNR_TH2[0]	00000100	04
254	FE	CSI Tx slave address	RW	CSI_TX_SLAVE_ADDR[6]	CSI_TX_SLAVE_ADDR[5]	CSI_TX_SLAVE_ADDR[4]	CSI_TX_SLAVE_ADDR[3]	CSI_TX_SLAVE_ADDR[2]	CSI_TX_SLAVE_ADDR[1]	CSI_TX_SLAVE_ADDR[0]		00000000	00



To access the registers listed in Table 92, SUB\_USR\_EN in Register Address 0x0E must be programmed to 10b. All read only registers are left blank.

**Table 92. User Sub Map 2 Register Map Details**

Address		Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	(Hex)
Dec	Hex												
128	80	ACE Control 1	RW	ACE_ENABLE								00000000	00
131	83	ACE Control 4	RW				ACE_LUMA_GAIN[4]	ACE_LUMA_GAIN[3]	ACE_LUMA_GAIN[2]	ACE_LUMA_GAIN[1]	ACE_LUMA_GAIN[0]	00001101	0D
132	84	ACE Control 5	RW	ACE_CHROMA_MAX[3]	ACE_CHROMA_MAX[2]	ACE_CHROMA_MAX[1]	ACE_CHROMA_MAX[0]	ACE_CHROMA_GAIN[3]	ACE_CHROMA_GAIN[2]	ACE_CHROMA_GAIN[1]	ACE_CHROMA_GAIN[0]	10001000	88
133	85	ACE Control 6	RW	ACE_RESPONSE_SPEED[3]	ACE_RESPONSE_SPEED[2]	ACE_RESPONSE_SPEED[2]	ACE_RESPONSE_SPEED[1]	ACE_GAMMA_GAIN[3]	ACE_GAMMA_GAIN[2]	ACE_GAMMA_GAIN[1]	ACE_GAMMA_GAIN[0]	11111000	F8
146	92	Dither control	RW								BR_DITHER_MODE	00000000	00
217	D9	Min Max 0	RW	MIN_THRESH_Y[7]	MIN_THRESH_Y[6]	MIN_THRESH_Y[5]	MIN_THRESH_Y[4]	MIN_THRESH_Y[3]	MIN_THRESH_Y[2]	MIN_THRESH_Y[1]	MIN_THRESH_Y[0]	00000000	00
218	DA	Min Max 1	RW	MAX_THRESH_Y[7]	MAX_THRESH_Y[6]	MAX_THRESH_Y[5]	MAX_THRESH_Y[4]	MAX_THRESH_Y[3]	MAX_THRESH_Y[2]	MAX_THRESH_Y[1]	MAX_THRESH_Y[0]	11111111	FF
219	DB	Min Max 2	RW	MIN_THRESH_C[7]	MIN_THRESH_C[6]	MIN_THRESH_C[5]	MIN_THRESH_C[4]	MIN_THRESH_C[3]	MIN_THRESH_C[2]	MIN_THRESH_C[1]	MIN_THRESH_C[0]	00000000	00
220	DC	Min Max 3	RW	MAX_THRESH_C[7]	MAX_THRESH_C[6]	MAX_THRESH_C[5]	MAX_THRESH_C[4]	MAX_THRESH_C[3]	MAX_THRESH_C[2]	MAX_THRESH_C[1]	MAX_THRESH_C[0]	11111111	FF
221	DD	Min Max 4	RW	MIN_SAMPLES_ALLOWED_Y[3]	MIN_SAMPLES_ALLOWED_Y[2]	MIN_SAMPLES_ALLOWED_Y[1]	MIN_SAMPLES_ALLOWED_Y[0]	MAX_SAMPLES_ALLOWED_Y[3]	MAX_SAMPLES_ALLOWED_Y[2]	MAX_SAMPLES_ALLOWED_Y[1]	MAX_SAMPLES_ALLOWED_Y[0]	11001100	CC
222	DE	Min Max 5	RW	MIN_SAMPLES_ALLOWED_C[3]	MIN_SAMPLES_ALLOWED_C[2]	MIN_SAMPLES_ALLOWED_C[1]	MIN_SAMPLES_ALLOWED_C[0]	MAX_SAMPLES_ALLOWED_C[3]	MAX_SAMPLES_ALLOWED_C[2]	MAX_SAMPLES_ALLOWED_C[1]	MAX_SAMPLES_ALLOWED_C[0]	11001100	CC
224	E0	FL control	RW								FL_ENABLE	00000000	00
225	E1	Y Average 0	RW	LINE_START[8]	LINE_START[7]	LINE_START[6]	LINE_START[5]	LINE_START[4]	LINE_START[3]	LINE_START[2]	LINE_START[1]	0001001	11
226	E2	Y Average 1	RW	LINE_END[8]	LINE_END[7]	LINE_END[6]	LINE_END[5]	LINE_END[4]	LINE_END[3]	LINE_END[2]	LINE_END[1]	10001000	88
227	E3	Y Average 2	RW	SAMPLE_START[9]	SAMPLE_START[8]	SAMPLE_START[7]	SAMPLE_START[6]	SAMPLE_START[5]	SAMPLE_START[4]	SAMPLE_START[3]	SAMPLE_START[2]	00010111	1B
228	E4	Y Average 3	RW	SAMPLE_END[9]	SAMPLE_END[8]	SAMPLE_END[7]	SAMPLE_END[6]	SAMPLE_END[5]	SAMPLE_END[4]	SAMPLE_END[3]	SAMPLE_END[2]	11010111	D7
229	E5	Y Average 4	RW	SAMPLE_END[1]	SAMPLE_END[0]	SAMPLE_START[1]	SAMPLE_START[0]			LINE_END[0]	LINE_START[0]	00100011	23
230	E6	Y Average 5	RW				Y_AVG_TIME_CONST[2]	Y_AVG_TIME_CONST[1]	Y_AVG_TIME_CONST[0]	Y_AVG_FILT_EN	CAPTURE_VALUE	00010000	10
231	E7	Y average data MSB	R	Y_AVERAGE[9]	Y_AVERAGE[8]	Y_AVERAGE[7]	Y_AVERAGE[6]	Y_AVERAGE[5]	Y_AVERAGE[4]	Y_AVERAGE[3]	Y_AVERAGE[2]		
232	E8	Y average data LSB	R							Y_AVERAGE[1]	Y_AVERAGE[0]		

To access the registers listed in Table 93, SUB\_USR\_EN in Register Address 0x0E must be programmed to 01b. All read only registers are left blank.

Table 93. Interrupt/VDP Map Details<sup>1</sup>

Address		Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	(Hex)
Dec	Hex												
64	40	Interrupt Configuration 1	RW	INTRQ_DUR_SEL[1]	INTRQ_DUR_SEL[0]	MV_INTRQ_SEL[1]	MV_INTRQ_SEL[0]		MPU_STIM_INTRQ	INTRQ_OP_SEL[1]	INTRQ_OP_SEL[0]	0001x000	10
66	42	Interrupt Status 1	R		MV_PS_CS_Q	SD_FR_CHNG_Q				SD_UNLOCK_Q	SD_LOCK_Q		
67	43	Interrupt Clear 1	W		MV_PS_CS_CLR	SD_FR_CHNG_CLR				SD_UNLOCK_CLR	SD_LOCK_CLR	x0000000	00
68	44	Interrupt Mask 1	RW		MV_PS_CS_MSKB <sup>2</sup>	SD_FR_CHNG_MSKB <sup>2</sup>				SD_UNLOCK_MSKB <sup>2</sup>	SD_LOCK_MSKB <sup>2</sup>	x00000000	00
69	45	Raw Status 2	R	MPU_STIM_INTRQ		CHX_MIN_MAX_INTRQ	EVEN_FIELD					CCAPD	
70	46	Interrupt Status 2	R	MPU_STIM_INTRQ_Q			SD_FIELD_CHNGD_Q					CCAPD_Q	
71	47	Interrupt Clear 2	W	MPU_STIM_INTRQ_CLR		CHX_MIN_MAX_INTRQ_CLR	SD_FIELD_CHNGD_CLR					CCAPD_CLR	0xx00000
72	48	Interrupt Mask 2	RW	MPU_STIM_INTRQ_MSKB <sup>2</sup>		CHX_MIN_MAX_INTRQ_MSKB <sup>2</sup>	SD_FIELD_CHNGD_MSKB <sup>2</sup>					CCAPD_MSKB <sup>2</sup>	0xx00000
73	49	Raw Status 3	R				SCM_LOCK		SD_H_LOCK	SD_V_LOCK	SD_OP_50Hz		
74	4A	Interrupt Status 3	R			PAL_SW_LK_CHNG_Q	SCM_LOCK_CHNG_Q	SD_AD_CHNG_Q	SD_H_LOCK_CHNG_Q	SD_V_LOCK_CHNG_Q	SD_OP_CHNG_Q		
75	4B	Interrupt Clear 3	W			PAL_SW_LK_CHNG_CLR	SCM_LOCK_CHNG_CLR	SD_AD_CHNG_CLR	SD_H_LOCK_CHNG_CLR	SD_V_LOCK_CHNG_CLR	SD_OP_CHNG_CLR	xx000000	00
76	4C	Interrupt Mask 3	RW			PAL_SW_LK_CHNG_MSKB <sup>2</sup>	SCM_LOCK_CHNG_MSKB <sup>2</sup>	SD_AD_CHNG_MSKB <sup>2</sup>	SD_H_LOCK_CHNG_MSKB <sup>2</sup>	SD_V_LOCK_CHNG_MSKB <sup>2</sup>	SD_OP_CHNG_MSKB <sup>2</sup>	xx000000	00
78	4E	Interrupt Status 4	R						VDP_CGMS_WSS_CHNGD_Q		VDP_CCAPD_Q		
79	4F	Interrupt Clear 4	W						VDP_CGMS_WSS_CHNGD_CLR		VDP_CCAPD_CLR	00x0x0x0	00
80	50	Interrupt Mask 4	RW						VDP_CGMS_WSS_CHNGD_MSKB <sup>2</sup>		VDP_CCAPD_MSKB <sup>2</sup>	00x0x0x0	00
81	51	Interrupt Latch 0	R			Y_CHANNEL_MIN_VIOLATION	Y_CHANNEL_MAX_VIOLATION	CB_CHANNEL_MIN_VIOLATION	CB_CHANNEL_MAX_VIOLATION	CR_CHANNEL_MIN_VIOLATION	CR_CHANNEL_MAX_VIOLATION		
96	60	VDP_CONFIG_1	RW					WST_PKT_DECODE_DISABLE	VDP_TTXT_TYPE_MAN_ENABLE	VDP_TTXT_TYPE_MAN[1]	VDP_TTXT_TYPE_MAN[0]	10001000	88
98	62	VDP_ADF_CONFIG_1	RW	ADF_ENABLE	ADF_MODE[1]	ADF_MODE[0]	ADF_DID[4]	ADF_DID[3]	ADF_DID[2]	ADF_DID[1]	ADF_DID[0]	00010101	15
99	63	VDP_ADF_CONFIG_2	RW	DUPLICATE_ADF		ADF_SDID[5]	ADF_SDID[4]	ADF_SDID[3]	ADF_SDID[2]	ADF_SDID[1]	ADF_SDID[0]	0x101010	2A
100	64	VDP_LINE_00E	RW	MAN_LINE_PGM				VBI_DATA_P318[3]	VBI_DATA_P318[2]	VBI_DATA_P318[1]	VBI_DATA_P318[0]	0xxx0000	00
101	65	VDP_LINE_00F	RW	VBI_DATA_P6_N23[3]	VBI_DATA_P6_N23[2]	VBI_DATA_P6_N23[1]	VBI_DATA_P6_N23[0]	VBI_DATA_P319_N286[3]	VBI_DATA_P319_N286[2]	VBI_DATA_P319_N286[1]	VBI_DATA_P319_N286[0]	00000000	00
102	66	VDP_LINE_010	RW	VBI_DATA_P7_N24[3]	VBI_DATA_P7_N24[2]	VBI_DATA_P7_N24[1]	VBI_DATA_P7_N24[0]	VBI_DATA_P320_N287[3]	VBI_DATA_P320_N287[2]	VBI_DATA_P320_N287[1]	VBI_DATA_P320_N287[0]	00000000	00
103	67	VDP_LINE_011	RW	VBI_DATA_P8_N25[3]	VBI_DATA_P8_N25[2]	VBI_DATA_P8_N25[1]	VBI_DATA_P8_N25[0]	VBI_DATA_P321_N288[3]	VBI_DATA_P321_N288[2]	VBI_DATA_P321_N288[1]	VBI_DATA_P321_N288[0]	00000000	00
104	68	VDP_LINE_012	RW	VBI_DATA_P9[3]	VBI_DATA_P9[2]	VBI_DATA_P9[1]	VBI_DATA_P9[0]	VBI_DATA_P322[3]	VBI_DATA_P322[2]	VBI_DATA_P322[1]	VBI_DATA_P322[0]	00000000	00
105	69	VDP_LINE_013	RW	VBI_DATA_P10[3]	VBI_DATA_P10[2]	VBI_DATA_P10[1]	VBI_DATA_P10[0]	VBI_DATA_P323[3]	VBI_DATA_P323[2]	VBI_DATA_P323[1]	VBI_DATA_P323[0]	00000000	00
106	6A	VDP_LINE_014	RW	VBI_DATA_P11[3]	VBI_DATA_P11[2]	VBI_DATA_P11[1]	VBI_DATA_P11[0]	VBI_DATA_P324_N272[3]	VBI_DATA_P324_N272[2]	VBI_DATA_P324_N272[1]	VBI_DATA_P324_N272[0]	00000000	00
107	6B	VDP_LINE_015	RW	VBI_DATA_P12_N10[3]	VBI_DATA_P12_N10[2]	VBI_DATA_P12_N10[1]	VBI_DATA_P12_N10[0]	VBI_DATA_P325_N273[3]	VBI_DATA_P325_N273[2]	VBI_DATA_P325_N273[1]	VBI_DATA_P325_N273[0]	00000000	00
108	6C	VDP_LINE_016	RW	VBI_DATA_P13_N11[3]	VBI_DATA_P13_N11[2]	VBI_DATA_P13_N11[1]	VBI_DATA_P13_N11[0]	VBI_DATA_P326_N274[3]	VBI_DATA_P326_N274[2]	VBI_DATA_P326_N274[1]	VBI_DATA_P326_N274[0]	00000000	00
109	6D	VDP_LINE_017	RW	VBI_DATA_P14_N12[3]	VBI_DATA_P14_N12[2]	VBI_DATA_P14_N12[1]	VBI_DATA_P14_N12[0]	VBI_DATA_P327_N275[3]	VBI_DATA_P327_N275[2]	VBI_DATA_P327_N275[1]	VBI_DATA_P327_N275[0]	00000000	00
110	6E	VDP_LINE_018	RW	VBI_DATA_P15_N13[3]	VBI_DATA_P15_N13[2]	VBI_DATA_P15_N13[1]	VBI_DATA_P15_N13[0]	VBI_DATA_P328_N276[3]	VBI_DATA_P328_N276[2]	VBI_DATA_P328_N276[1]	VBI_DATA_P328_N276[0]	00000000	00
111	6F	VDP_LINE_019	RW	VBI_DATA_P16_N14[3]	VBI_DATA_P16_N14[2]	VBI_DATA_P16_N14[1]	VBI_DATA_P16_N14[0]	VBI_DATA_P329_N277[3]	VBI_DATA_P329_N277[2]	VBI_DATA_P329_N277[1]	VBI_DATA_P329_N277[0]	00000000	00
112	70	VDP_LINE_01A	RW	VBI_DATA_P17_N15[3]	VBI_DATA_P17_N15[2]	VBI_DATA_P17_N15[1]	VBI_DATA_P17_N15[0]	VBI_DATA_P330_N278[3]	VBI_DATA_P330_N278[2]	VBI_DATA_P330_N278[1]	VBI_DATA_P330_N278[0]	00000000	00
113	71	VDP_LINE_01B	RW	VBI_DATA_P18_N16[3]	VBI_DATA_P18_N16[2]	VBI_DATA_P18_N16[1]	VBI_DATA_P18_N16[0]	VBI_DATA_P331_N279[3]	VBI_DATA_P331_N279[2]	VBI_DATA_P331_N279[1]	VBI_DATA_P331_N279[0]	00000000	00
114	72	VDP_LINE_01C	RW	VBI_DATA_P19_N17[3]	VBI_DATA_P19_N17[2]	VBI_DATA_P19_N17[1]	VBI_DATA_P19_N17[0]	VBI_DATA_P332_N280[3]	VBI_DATA_P332_N280[2]	VBI_DATA_P332_N280[1]	VBI_DATA_P332_N280[0]	00000000	00
115	73	VDP_LINE_01D	RW	VBI_DATA_P20_N18[3]	VBI_DATA_P20_N18[2]	VBI_DATA_P20_N18[1]	VBI_DATA_P20_N18[0]	VBI_DATA_P333_N281[3]	VBI_DATA_P333_N281[2]	VBI_DATA_P333_N281[1]	VBI_DATA_P333_N281[0]	00000000	00
116	74	VDP_LINE_01E	RW	VBI_DATA_P21_N19[3]	VBI_DATA_P21_N19[2]	VBI_DATA_P21_N19[1]	VBI_DATA_P21_N19[0]	VBI_DATA_P334_N282[3]	VBI_DATA_P334_N282[2]	VBI_DATA_P334_N282[1]	VBI_DATA_P334_N282[0]	00000000	00

Address		Register Name	RW	7	6	5	4	3	2	1	0	Reset Value	(Hex)
Dec	Hex												
117	75	VDP_LINE_01F	RW	VBI_DATA_P22_N20[3]	VBI_DATA_P22_N20[2]	VBI_DATA_P22_N20[1]	VBI_DATA_P22_N20[0]	VBI_DATA_P335_N283[3]	VBI_DATA_P335_N283[2]	VBI_DATA_P335_N283[1]	VBI_DATA_P335_N283[0]	00000000	00
118	76	VDP_LINE_020	RW	VBI_DATA_P23_N21[3]	VBI_DATA_P23_N21[2]	VBI_DATA_P23_N21[1]	VBI_DATA_P23_N21[0]	VBI_DATA_P336_N284[3]	VBI_DATA_P336_N284[2]	VBI_DATA_P336_N284[1]	VBI_DATA_P336_N284[0]	00000000	00
119	77	VDP_LINE_021	RW	VBI_DATA_P24_N22[3]	VBI_DATA_P24_N22[2]	VBI_DATA_P24_N22[1]	VBI_DATA_P24_N22[0]	VBI_DATA_P337_N285[3]	VBI_DATA_P337_N285[2]	VBI_DATA_P337_N285[1]	VBI_DATA_P337_N285[0]	00000000	00
120	78	VDP_STATUS	R	TTXT_AVL					CGMS_WSS_AVL	CC_EVEN_FIELD	CC_AVL		
120	78	VDP_STATUS_CLEAR	W						CGMS_WSS_CLEAR		CC_CLEAR	00000000	00
121	79	VDP_CCAP_DATA_0	R	CCAP_BYTE_1[7]	CCAP_BYTE_1[6]	CCAP_BYTE_1[5]	CCAP_BYTE_1[4]	CCAP_BYTE_1[3]	CCAP_BYTE_1[2]	CCAP_BYTE_1[1]	CCAP_BYTE_1[0]		
122	7A	VDP_CCAP_DATA_1	R	CCAP_BYTE_2[7]	CCAP_BYTE_2[6]	CCAP_BYTE_2[5]	CCAP_BYTE_2[4]	CCAP_BYTE_2[3]	CCAP_BYTE_2[2]	CCAP_BYTE_2[1]	CCAP_BYTE_2[0]		
125	7D	VDP_CGMS_WSS_DATA_0	R					CGMS_CRC[5]	CGMS_CRC[4]	CGMS_CRC[3]	CGMS_CRC[2]		
126	7E	VDP_CGMS_WSS_DATA_1	R	CGMS_CRC[1]	CGMS_CRC[0]	CGMS_WSS[13]	CGMS_WSS[12]	CGMS_WSS[11]	CGMS_WSS[10]	CGMS_WSS[9]	CGMS_WSS[8]		
127	7F	VDP_CGMS_WSS_DATA_2	R	CGMS_WSS[7]	CGMS_WSS[6]	CGMS_WSS[5]	CGMS_WSS[4]	CGMS_WSS[3]	CGMS_WSS[2]	CGMS_WSS[1]	CGMS_WSS[0]		
156	9C	VDP_OUTPUT_SEL	RW				WSS_CGMS_CB_CHANGE					00110000	30

<sup>1</sup> x in a reset value indicates do not care.

<sup>2</sup> B at the end of the bit name equals an overbar for the whole bit name.

To access all the registers listed in Table 94, SUB\_USR\_EN in Register Address 0x0E must be programmed to 00b. The gray shading is the default.

Table 94. Register Map Descriptions (Main Register Map)<sup>1</sup>

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes
			7	6	5	4	3	2	1	0		
0x00	Input control	INSEL[4:0]; the INSEL bits allow the user to select an input channel and the input format	0	0	0	0	0	0	0	0	CVBS input on A <sub>IN</sub> 1	
			0	0	0	0	0	0	1	0	CVBS input on A <sub>IN</sub> 2	
			0	0	0	0	1	0	0	0	CVBS input on A <sub>IN</sub> 3	
			0	0	0	0	1	1	0	0	CVBS input on A <sub>IN</sub> 4	
			0	1	0	0	0	0	0	0	Y input on A <sub>IN</sub> 1, C input on A <sub>IN</sub> 2	
			0	1	0	0	0	0	1	0	Y input on A <sub>IN</sub> 3, C input on A <sub>IN</sub> 4	
			0	1	1	0	0	0	0	0	Y input on A <sub>IN</sub> 1, Pb input on A <sub>IN</sub> 2, Pr input on A <sub>IN</sub> 3	
			0	1	1	1	1	0	0	0	Differential positive on A <sub>IN</sub> 1, differential negative on A <sub>IN</sub> 2	
0x01	Video Selection 1	Reserved					0	0	0	Sets to default		
		ENVSPROC				0				Disables VSYNC processor		
						1				Enables VSYNC processor		
		Reserved			0					Sets to default		
		BETACAM; enables BETACAM levels			0					Standard video input		
		ENHSPLL		0						Disables HSYNC processor		
				1						Enables HSYNC processor		
0x02	Video Selection 2	Reserved				0	1	0	0	Set to default		
		VID_SEL[3:0]; the VID_SEL bits allow the user to select the input video standard	0	0	0	0						Autodetects PAL B/PAL G/PAL H/PAL I/PAL D, NTSC J (no pedestal), SECAM
			0	0	0	1						Autodetects PAL B/PAL G/PAL H/PAL I/PAL D, NTSC M (pedestal), SECAM
			0	0	1	0						Autodetects PAL N (pedestal), NTSC J (no pedestal), SECAM
			0	0	1	1						Autodetects PAL N (pedestal), NTSC M (pedestal) SECAM
			0	1	0	0						NTSC J
			0	1	0	1						NTSC M
			0	1	1	0						PAL 60
			0	1	1	1						NTSC 4.43
			1	0	0	0						PAL B/G/H/I/D
			1	0	0	1						PAL N = PAL B/PAL G/PAL H/PAL I/PAL D (with pedestal)
			1	0	1	0						PAL M (without pedestal)
			1	0	1	1						PAL M
			1	1	0	0						PAL Combination N
			1	1	0	1						PAL Combination N (with pedestal)
	1	1	1	0					SECAM			
	1	1	1	1					SECAM			
0x03	Output control	Reserved			0	0	1	1	0	0	Reserved	See also TIM_OE and TRI_LLC
		TOD; tristate output drivers; this bit allows the user to tristate the output drivers; pixel outputs, HS and VS/FIELD/SFL		0							Output drivers enabled	
				1							Output drivers tristated	
		VBI_EN; vertical blanking interval data enable; allows VBI data (Line 1 to Line 21) to be passed through with only a minimum amount of filtering performed	0								All lines filtered and scaled	
		1								Only active video region filtered		

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes			
			7	6	5	4	3	2	1	0					
0x04	Extended output control	Range; allows the user to select the range of output values; can be ITU-R BT.656 compliant or can fill the whole accessible number range									0	16 ≤ Y ≤ 235, 16 ≤ C/P ≤ 240	ITU-R BT.656		
											1	1 ≤ Y ≤ 254, 1 ≤ C/P ≤ 254	Extended range		
		EN_SFL_PIN									0	Disables SFL output	SFL output enables encoder and decoder to be connected directly		
											1	Outputs SFL information on the SFL pin			
		BL_C_VBI; blank chroma during VBI; if set, it enables data in the VBI region to be passed through the decoder undistorted									0	Decode and output color during VBI	during VBI		
											1	Blank Cr and Cb values during VBI			
		TIM_OE; enables timing signals output									0	HS, VS, FIELD tristated	Controlled by TOD		
									1	HS, VS, FIELD forced active					
Reserved															
BT.656-4; allows the user to select an output mode compatible with ITU-R BT.656-3/-4												ITU-R BT.656-3 compatible			
													ITU-R BT.656-4 compatible		
0x07	Autodetect enable	AD_PAL_EN; PAL B/PAL D/PAL I/PAL G/PAL H autodetect enable										0	Disables		
													1		Enables
		AD_NTSC_EN; NTSC autodetect enable										0	Disables		
												1	Enables		
		AD_PALM_EN; PAL M autodetect enable										0	Disables		
												1	Enables		
		AD_PALN_EN; PAL N autodetect enable										0	Disables		
												1	Enables		
		AD_P60_EN; PAL 60 autodetect enable										0	Disables		
										1	Enables				
AD_N443_EN; NTSC 4.43 autodetect enable										0	Disables				
										1	Enables				
AD_SECAM_EN; SECAM autodetect enable										0	Disables				
										1	Enables				
AD_SEC525_EN; SECAM 525 autodetect enable										0	Disables				
										1	Enables				
0x08	Contrast	CON[7:0]; contrast adjust; this is the user control for contrast adjustment	1	0	0	0	0	0	0	0	0	Luma gain = 1	0x00 gain = 0, 0x80 gain = 1, 0xFF gain = 2		
0x0A	Brightness Adjust	BRI[7:0]; this register controls the brightness of the video signal	0	0	0	0	0	0	0	0	0		0x00 = 0 IRE, 0x7F = +30 IRE, 0x80 = -30 IRE		
0x0B	Hue Adjust	HUE[7:0]; this register contains the value for the color hue adjustment	0	0	0	0	0	0	0	0	0		Hue range = -90° to +90°		
0x0C	Default Value Y	DEF_VAL_EN; default value enable										0	Free-run mode dependent on DEF_VAL_AUTO_EN		
													1	Forces free-run mode on	
		DEF_VAL_AUTO_EN; default value automatic enable											0	Disables free-run mode	When lock is lost, free-run mode can be enabled to output stable timing, clock, and a set color
													1	Enables automatic free-run mode	
DEF_Y[5:0]; default value is Y; this register holds the Y default value													Y[7:0] = {DEF_Y[5:0], 0, 0}	Default Y value output in free-run mode	
0x0D	Default Value C	DEF_C[7:0]; default value is C; the Cr and Cb default values are defined in this register	0	1	1	1	1	1	1	0	0	Cr[3:0] = {DEF_C[7:4]}, Cb[3:0] = {DEF_C[3:0]}	Default Cb/Cr value output in free-run mode; default values give blue screen output		

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes	
			7	6	5	4	3	2	1	0			
0x0E	ADI Control 1	Reserved				0	0	0	0	0	Sets as default	See Figure 47	
		SUB_USR_EN[1:0]; enables user to access the interrupt/VDP map and User Sub Map 2		0	0						Accesses main register space		
				0	1						Accesses interrupt/VDP register space		
				1	0						Accesses User Sub Map 2		
		Reserved	0								Sets as default		
0x0F	Power management	Reserved							0	0	Sets to default		
		Reserved				0	0				Sets to default		
		PWRDWN; power-down places the decoder into a full power-down mode			0							System functional	
					1							Powered down	
		Reserved		0								Sets to default	
		Reset; chip reset, loads all I <sup>2</sup> C bits with default values	0									Normal operation	
			1									Starts reset sequence	Executing reset takes approximately 2 ms; this bit is self-clearing
0x10	Status 1 (read only)	IN_LOCK								x	1 = in lock (now)	Provides info about the internal status of the decoder	
		LOST_LOCK								x	1 = lost lock (since last read)		
		FSC_LOCK						x			1 = f <sub>sc</sub> lock (now)		
		FOLLOW_PW					x				1 = peak white AGC mode active		
		AD_RESULT[2:0]; autodetection result reports the standard of the input video		0	0	0						NTSC M/NTSC J	Detected standard
				0	0	1						NTSC 4.43	
				0	1	0						PAL M	
				0	1	1						PAL 60	
				1	0	0						PAL B/PAL G/PAL H/PAL I/PAL D	
				1	0	1						SECAM	
				1	1	0						PAL Combination N	
		1	1	1						SECAM 525			
	COL_KILL	x								1 = color kill is active	Color kill		
0x11	IDENT (read only)	IDENT[7:0]; provides ID on the revision of the part	0	0	0	1	1	1	0	0		Power-up value = 0x1C	
0x12	Status 2 (read only)	MVCS DET								x	MV color striping detected	1 = detected	
		MVCS T3								x	MV color striping type	0 = Type 2, 1 = Type 3	
		MV PS DET						x			MV pseudosync detected	1 = detected	
		MV AGC DET					x				MV AGC pulses detected	1 = detected	
		LL NSTD				x					Nonstandard line length	1 = detected	
		FSC NSTD			x						f <sub>sc</sub> frequency nonstandard	1 = detected	
		Reserved	x	x									
0x13	Status 3 (read only)	INST_HLOCK								x	1 = horizontal lock achieved	Unfiltered	
		Reserved								x	Reserved		
		SD_OP_50Hz						0			SD 60 Hz detected	SD field rate detect	
								1			SD 50 Hz detected		
		Reserved					x						
		FREE_RUN_ACT				x					1 = free-run mode active		
		STD FLD LEN			x						1 = field length standard	Correct field length found	
		Interlaced		x							1 = interlaced video detected	Field sequence found	
PAL_SW_LOCK	x								1 = swinging burst detected	Reliable swinging burst sequence			

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes
			7	6	5	4	3	2	1	0		
0x14	Analog clamp control	FREE_RUN_PAT_SEL[2:0]						0	0	0	Single color set by DEF_C and DEF_Y; see Color Controls section	
							0	0	1	100% color bars		
							1	0	1	Boundary box		
		Reserved				0					Sets to default	
		CCLEN; current clamp enable allows the user to switch off the current sources in the analog front			0						Current sources switched off	
				1							Current sources enabled	
		Reserved	0	0	0						Sets to default	
0x15	Digital Clamp Control 1	Reserved				x	x	x	x	Sets to default		
		DCFE; digital clamp freeze enable			0					Digital clamp on		
				1						Digital clamp off		
		DCT[1:0]; digital clamp timing determines the time constant of the digital fine clamp circuitry	0	0								Slow (TC = 1 sec)
			0	1								Medium (TC = 0.5 sec)
			1	0								Fast (TC = 0.1 sec)
			1	1								TC dependent on video
Reserved	0								Set to default			
0x17	Shaping Filter Control 1	YSFM[4:0]; selects Y shaping filter mode in CVBS-only mode; allows the user to select a wide range of low-pass/notch filters; if either auto mode is selected, the decoder selects the optimum Y filter depending on the CVBS video source quality (good vs. poor)				0	0	0	0	0	Autowide notch for poor quality sources or wideband filter with comb for good quality input	Decoder selects optimum Y shaping filter depending on CVBS quality
					0	0	0	0	1	1	Autonarrow notch for poor quality sources or wideband filter with comb for good quality input	
					0	0	0	1	0	0	SVHS 1	If one of these modes is selected, the decoder does not change filter modes; depending on video quality, a fixed filter response (the one selected) is used for good and bad quality video
					0	0	0	1	1	1	SVHS 2	
					0	0	1	0	0	0	SVHS 3	
					0	0	1	0	1	1	SVHS 4	
					0	0	1	1	0	0	SVHS 5	
					0	0	1	1	1	1	SVHS 6	
					0	1	0	0	0	0	SVHS 7	
					0	1	0	0	1	1	SVHS 8	
					0	1	0	1	0	0	SVHS 9	
					0	1	0	1	1	1	SVHS 10	
					0	1	1	0	0	0	SVHS 11	
					0	1	1	0	1	1	SVHS 12	
					0	1	1	1	0	0	SVHS 13	
					0	1	1	1	1	1	SVHS 14	
					1	0	0	0	0	0	SVHS 15	
					1	0	0	0	1	1	SVHS 16	
					1	0	0	1	0	0	SVHS 17	
					1	0	0	1	1	1	SVHS 18 (CCIR 601)	
					1	0	1	0	0	0	PAL NN1	
					1	0	1	0	1	1	PAL NN2	
					1	0	1	1	0	0	PAL NN3	
					1	0	1	1	1	1	PAL WN1	
					1	1	0	0	0	0	PAL WN2	
					1	1	0	0	1	1	NTSC NN1	
					1	1	0	1	0	0	NTSC NN2	
					1	1	0	1	1	1	NTSC NN3	
					1	1	1	0	0	0	NTSC WN1	
			1	1	1	0	1	1	NTSC WN2			
			1	1	1	1	1	0	NTSC WN3			
			1	1	1	1	1	1	Reserved			

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes			
			7	6	5	4	3	2	1	0					
		CSFM[2:0]: C shaping filter mode allows selection from a range of low-pass chrominance filters; if either auto mode is selected, the decoder selects the optimum C filter depending on the CVBS video source quality (good vs. bad); nonauto settings force a C filter for all standards and quality of CVBS video	0	0	0							Autoselection 1.5 MHz	Automatically selects a C filter based on video standard and quality  Selects a C filter for all video standards and for good and bad video		
			0	0	1									Autoselection 2.17 MHz	
			0	1	0									SH1	
			0	1	1									SH2	
			1	0	0									SH3	
			1	0	1									SH4	
			1	1	0									SH5	
			1	1	1									Wideband mode	
0x18	Shaping Filter Control 2	WYSFM[4:0]; wideband Y shaping filter mode allows the user to select which Y shaping filter is used for the Y component of Y/C, YPrPb, B/W input signals; it is also used when a good quality input CVBS signal is detected; for all other inputs, the Y shaping filter chosen is controlled by YSFM[4:0]				0	0	0	0	0		Reserved, do not use			
						0	0	0	0	1	0			Reserved, do not use	
						0	0	0	1	0					SVHS 1
						0	0	0	1	1					SVHS 2
						0	0	1	0	0					SVHS 3
						0	0	1	0	1					SVHS 4
						0	0	1	1	0					SVHS 5
						0	0	1	1	1					SVHS 6
						0	1	0	0	0					SVHS 7
						0	1	0	0	1					SVHS 8
						0	1	0	1	0					SVHS 9
						0	1	0	1	1					SVHS 10
						0	1	1	0	0					SVHS 11
						0	1	1	0	1					SVHS 12
						0	1	1	1	0					SVHS 13
						0	1	1	1	1					SVHS 14
						1	0	0	0	0					SVHS 15
						1	0	0	0	1					SVHS 16
						1	0	0	1	0					SVHS 17
						1	0	0	1	1					SVHS 18 (CCIR 601)
			1	0	1	0	0				Reserved, do not use				
			~	~	~	~	~				Reserved, do not use				
			1	1	1	1	1				Reserved, do not use				
	Reserved		0	0							Set to default				
	WYSFMOVR; enables use of the automatic WYSFM filter	0									Autoselection of best filter				
		1									Manual select filter using WYSFM[4:0]				
0x19	Comb filter control	PSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (PAL)							0	0		Narrow			
									0	1		Medium			
										1	0			Wide	
										1	1			Widest	
		NSFSEL[1:0]; controls the signal bandwidth that is fed to the comb filters (NTSC)					0	0						Narrow	
							0	1						Medium	
							1	0						Medium	
							1	1						Wide	
	Reserved	1	1	1	1										
0x1D	ADI Control 2	Reserved			0	0	0	0	x	x	x				
		Reserved		1											
		TRI_LLC; tristate LLC driver	0										LLC pin active		
		1										LLC pin tristated			



Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes		
			7	6	5	4	3	2	1	0				
0x27	Pixel delay control	LTA[1:0]; luma timing adjust allows the user to specify a timing difference between chroma and luma samples							0	0	No delay	CVBS mode, LTA[1:0] = 00b, Y/C mode, LTA[1:0] = 01b, YPrPb mode, LTA[1:0] = 01b		
									0	1	Luma one clock (37 ns) late			
									1	0	Luma two clocks (74 ns) early			
									1	1	Luma one clock (37 ns) early			
		Reserved						0			Sets to 0			
		CTA[2:0]; chroma timing adjust allows a specified timing difference between the luma and chroma samples			0	0	0						Reserved	CVBS mode CTA[2:0] = 011b, Y/C mode, CTA[2:0] = 101b, YPrPb mode, CTA[2:0] = 110b
					0	0	1						Chroma + two pixels (early)	
					0	1	0						Chroma + one pixel (early)	
					0	1	1						No delay	
					1	0	0						Chroma – one pixel (late)	
					1	0	1						Chroma – two pixels (late)	
					1	1	0						Chroma – three pixels (late)	
		AUTO_PDC_EN; automatic programmed delay control. automatically programs the LTA/CTA values so that luma and chroma are aligned at the output for all modes of operation			0								Use values in LTA[1:0] and CTA[2:0] for delaying luma/chroma	
					1								LTA and CTA values determined automatically	
SWPC; allows the Cr and Cb samples to be swapped	0										No swapping			
	1									Swaps the Cr and Cb output samples				
0x2B	Misc gain control	PW_UPD; peak white update determines the rate of gain							0	Updates once per video line	Peak white must be enabled; see LAGC[2:0]			
									1	Updates once per field				
		Reserved			1	0	0	0	0	Sets to default				
		CKE; color kill enable allows the color kill function to be switched on and off	0									Color kill disabled		
			1									Color kill enabled		
Reserved	1								Sets to default					
0x2C	AGC mode control	CAGC[1:0]; chroma automatic gain control selects the basic mode of operation for the AGC in the chroma path							0	0	Manual fixed gain	Use CMG[11:0]		
									0	1	Uses luma gain for chroma			
									1	0	Automatic gain			
									1	1	Freeze chroma gain			
		Reserved					1	1			Sets to 1			
		LAGC[2:0]; luma automatic gain control selects the mode of operation for the gain control in the luma path	0	0	0						Manual fixed gain	Uses LMG[11:0]		
			0	0	1						AGC peak white algorithm off			
			0	1	0						AGC peak white algorithm on			
			0	1	1						Reserved			
			1	0	0						Reserved			
			1	0	1						Reserved			
			1	1	0						Reserved			
		1	1	1						Freeze gain				
		Reserved	1							Sets to 1				
0x2D	Chroma Gain Control 1, Chroma Gain 1 (CG)	CMG[11:8]/CG[11:8]; in manual mode, the chroma gain control can be used to program a desired manual chroma gain; in auto mode, it can be used to read back the current gain value					0	1	0	0		CAGC[1:0] settings decide in which mode CMG[11:0] operates		
			Reserved			1	1						Set to 1	
			CAGT[1:0]; chroma automatic gain timing allows adjustment of the chroma AGC tracking speed	0	0								Slow (TC = 2 sec)	
				0	1								Medium (TC = 1 sec)	
		1		0							Reserved			
1	1							Adaptive						
0x2E	Chroma Gain Control 2, Chroma Gain 2 (CG)	CMG[7:0]/CG[7:0]; chroma manual gain lower eight bits; see CMG[11:8]/CG[11:8] for description	0	0	0	0	0	0	0	0	CMG[11:0] = see the CMG section	Minimum value = 0d, maximum value = 4095d		

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes	
			7	6	5	4	3	2	1	0			
0x2F	Luma Gain Control 1, Luma Gain 1 (LG)	LMG[11:8]/LG[11:8]; in manual mode, luma gain control can be used to program a desired manual luma gain; in auto mode, it can be used to read back the actual gain value used					x	x	x	x	LAGC[1:0] settings decide in which mode LMG[11:0] operates		
		Reserved			1	1					Sets to 1		
		LAGT[1:0]; luma automatic gain timing allows adjustment of the luma AGC tracking speed	0	0									Slow (TC = 2 sec)
			0	1									Medium (TC = 1 sec)
			1	0									Fast (TC = 0.2 sec)
1	1									Adaptive			
0x30	Luma Gain Control 2, Luma Gain 2 (LG)	LMG[7:0]/LG[7:0]; luma manual gain/ luma gain lower eight bits; see LMG[11:8]/LG[11:8] for description	x	x	x	x	x	x	x	LMG[7:0]/LG[7:0]; luma manual gain/luma gain lower eight bits; see LMG[11:8]/LG[11:8] for description	Minimum value = 1024d, Maximum value = 4095d		
0x31	VS/FIELD Control 1	Reserved						0	1	0	Sets to default		
		HVSTIM; horizontal VSYNC timing; selects where within a line of video the VSYNC signal is asserted					0				Start of line relative to HSE		HSE = HSYNC end
							1				Start of line relative to HSB		HSB = HSYNC begin
		NEWAVMODE; sets the EAV/SAV mode				0							EAV/SAV codes generated to suit Analog Devices encoders
						1							Manual VS/FIELD position controlled by the Register 0x32, Register 0x33, and Register 0xE5 to Register 0xEA
Reserved	0	0	0							Sets to default			
0x32	VS/FIELD Control 2	Reserved			0	0	0	0	0	1	Sets to default	NEWAVMODE bit must be set high	
		VSBHE		0							VSYNC signal goes high in the middle of the line (even field)		
				1							VSYNC signal changes state at the start of the line (even field)		
		VSBHO	0								VSYNC signal goes high in the middle of the line (odd field)		
			1								VSYNC signal changes state at the start of the line (odd field)		
0x33	VS/FIELD Control 3	Reserved			0	0	0	1	0	0	Sets to default	NEWAVMODE bit must be set high	
		VSEHE		0							VSYNC signal goes low in the middle of the line (even field)		
				1							VSYNC signal changes state at the start of the line (even field)		
		VSEHO	0								VSYNC signal goes low in the middle of the line (odd field)		
			1								VSYNC signal changes state at the start of the line odd field		
0x34	HS Position Control 1	HSE[10:8]; HSYNC end allows positioning of the HSYNC output within the video line						0	0	0	HSYNC output ends HSE[10:0] pixels after the falling edge of HSYNC	Using HSB and HSE, the position/length of the output HSYNC can be programmed	
		Reserved					0				Sets to 0		
		HSB[10:8]; HSYNC begin allows positioning of the HSYNC output within the video line		0	0	0					HS output starts HSB[10:0] pixels after the falling edge of HSYNC		
		Reserved	0								Sets to 0		
0x35	HS Position Control 2	HSB[7:0]; see Address 0x34, using HSB[10:0] and HSE[10:0], users can program the position and length of the HSYNC output signal	0	0	0	0	0	0	1	0			
0x36	HS Position Control 3	HSE[7:0]; see Address 0x35 description	0	0	0	0	0	0	0	0			

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)							Comments	Notes		
			7	6	5	4	3	2	1			0	
0x37	Polarity	PCLK; sets polarity of LLC									0	Inverts polarity	
												1	
		Reserved						0	0			Set to 0	
		PF; sets the FIELD polarity					0						
		Reserved				0							
		PVS; sets the VSYNC polarity			0							Active high	
		Reserved			1							Active low	
		PHS; sets HSYNC polarity		0		0						Active high	
			1		1					Active low			
0x38	NTSC comb control	YCMN[2:0]; luma comb mode, NTSC						0	0	0	Adaptive three-line, three-tap luma comb		
								1	0	0	Uses low-pass/notch filter		
								1	0	1	Fixed luma comb two-line (two taps)		Top lines of memory
								1	1	0	Fixed luma comb three-line (three taps)		All lines of memory
		CCMN[2:0]; chroma comb mode, NTSC				0	0	0	Three-line adaptive for CTAPSN = 01, four-line adaptive for CTAPSN = 10, five-line adaptive for CTAPSN = 11				
					1	0	0	Disables chroma comb					
					1	0	1	Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Top lines of memory				
					1	1	0	Fixed three-line for CTAPSN = 01, fixed four-line for CTAPSN = 10, fixed five-line for CTAPSN = 11	All lines of memory				
		CTAPSN[1:0]; chroma comb taps, NTSC	0	0	Not used								
			0	1	Adapts three lines to two lines								
			1	0	Adapts five lines to three lines								
			1	1	Adapts five lines to four lines								
0x39	PAL comb control	YCMP[2:0]; luma comb mode, PAL						0	0	0	Adaptive five-line, three-tap luma comb		
								1	0	0	Use low-pass notch filter		
								1	0	1	Fixed luma comb (three-line)		Top lines of memory
								1	1	0	Fixed luma comb (five-line)		All lines of memory
		CCMP[2:0]; chroma comb mode, PAL				0	0	0	Three-line adaptive for CTAPSN = 01, four-line adaptive for CTAPSN = 10, five-line adaptive for CTAPSN = 11				
					1	0	0	Disable chroma comb					
					1	0	1	Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Top lines of memory				
					1	1	0	Fixed three-line for CTAPSN = 01, fixed four-line for CTAPSN = 10, fixed five-line for CTAPSN = 11	All lines of memory				
				1	1	1	Fixed two-line for CTAPSN = 01, fixed three-line for CTAPSN = 10, fixed four-line for CTAPSN = 11	Bottom lines of memory					

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes		
			7	6	5	4	3	2	1	0				
		CTAPSP[1:0]; chroma comb taps, PAL	0	0								Not used		
			0	1								Adapts five lines to three lines (two taps)		
			1	0								Adapts five lines to three lines (three taps)		
			1	1								Adapts five lines to four lines (four taps)		
0x3A	ADC control	MUX PDN override; mux power-down override									0		No control over power-down for muxes and associated channel circuit	
											1		Allows power-down of MUX0/MUX1/MUX2 and associated channel circuit; when INSEL[4:0] is used, unused channels are automatically powered down	
		PWRDWN_MUX_2; enables power-down of MUX2 and associated channel clamp and buffer									0		MUX2 and associated channel in normal operation	
											1		Power down MUX2 and associated channel operation	MUX PDN override = 1
		PWRDWN_MUX_1; enables power-down of MUX1 and associated channel clamp and buffer								0			MUX1 and associated channel in normal operation	
										1			Power down MUX1 and associated channel operation	MUX PDN override = 1
		PWRDWN_MUX_0; enables power-down of MUX0 and associated channel clamp and buffer							0				MUX0 and associated channel in normal operation	
							1				Power down MUX0 and associated channel operation	MUX PDN override = 1		
Reserved		0	0	0	0						Sets as default			
0x3D	Manual window control	Reserved					0	0	1	0		Sets to default		
		CKILLTHR[2:0]; color kill threshold		0	0	0							NTSC, PAL color kill at <0.5%, SECAM no color kill	CKE = 1 enables the color kill function and must be enabled for CKILLTHR[2:0] to take effect
				0	0	1							NTSC, PAL color kill at <1.5%, SECAM color kill at <5%	
				0	1	0							NTSC, PAL color kill at <2.5%, SECAM color kill at <7%	
				0	1	1							NTSC, PAL color kill at <4%, SECAM color kill at <8%	
				1	0	0							NTSC, PAL color kill at <8.5%, SECAM color kill at <9.5%	
				1	0	1							NTSC, PAL color kill at <16%, SECAM color kill at <15%	
				1	1	0							NTSC, PAL color kill at <32%, SECAM color kill at <32%	
		Reserved		1	1	1							Reserved	
Reserved	0										Sets to default			
0x41	Resample control	Reserved			0	0	0	0	0	0	1	Sets to default		
		SFL_INV; controls the behavior of the PAL switch bit		0									SFL-compatible with the ADV717x and ADV73xx video encoders	
				1									SFL-compatible with older video encoders such as the <a href="#">ADV7194</a> .	
Reserved	0										Set to default			

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes	
			7	6	5	4	3	2	1	0			
0x4D	CTI DNR Control 1	CTI_EN; CTI enable									0	Disables CTI	
											1	Enables CTI	
		CTI_AB_EN; enables the mixing of the transient improved chroma with the original signal									0	Disables CTI alpha blender	
											1	Enables CTI alpha blender	
		CTI_AB[1:0]; controls the behavior of the alpha-blend circuitry						0	0			Sharpest mixing between sharpened/original chroma signal	
								0	1			Sharp mixing between sharpened and original chroma signal	
								1	0			Smooth mixing between sharpened/original chroma signal	
								1	1			Smoothest mixing between sharpened and original chroma signal	
		Reserved				0					Sets to default		
DNR_EN; enables or bypasses the DNR block			0						Bypasses the DNR block				
			1						Enables the DNR block				
Reserved	1	1							Sets to default				
0x4E	CTI DNR Control 2	CTI_C_TH[7:0]; specifies how big the amplitude step must be to be steepened by the CTI block	0	0	0	0	1	0	0	0			
0x50	DNR Noise Threshold 1	DNR_TH[7:0]; specifies the maximum luma edge that is interpreted as noise and is therefore blanked	0	0	0	0	1	0	0	0			
0x51	Lock count	CIL[2:0]; count into lock determines the number of lines the system must remain in lock before showing a locked status						0	0	0	One line of video		
								0	0	1	Two lines of video		
								0	1	0	Five lines of video		
								0	1	1	10 lines of video		
								1	0	0	100 lines of video		
								1	0	1	500 lines of video		
								1	1	0	1000 lines of video		
								1	1	1	100,000 lines of video		
		COL[2:0]; count out of lock determines the number of lines the system must remain out-of-lock before showing a lost-locked status			0	0	0				One line of video		
					0	0	1				Two lines of video		
					0	1	0				Five lines of video		
					0	1	1				10 lines of video		
					1	0	0				100 lines of video		
					1	0	1				500 lines of video		
		SRLS; select raw lock signal and selects the determination of the lock status			1	1	0				1000 lines of video		
					1	1	1				100,000 lines of video		
			0							Over field with vertical info			
		FSCLE; f <sub>sc</sub> lock enable		0						Line-to-line evaluation			
			1							Lock status set only by horizontal lock			
		1						Lock status set by horizontal lock and subcarrier lock					
0x60	ADC Switch 3	MUX3[2:0]					0	0	0	0	No connect		
							0	0	0	1	No connect		
							0	0	1	0	A <sub>IN</sub> 2		
							0	0	1	1	No connect		
							0	1	0	0	A <sub>IN</sub> 4		
		Reserved	0	0	0	1	0						
0x6A	Output Sync Select 1	HS_OUT_SEL[2:0] selects which sync comes out on the HS pin					0	0	0	HSYNC			
							0	0	1	VSYNC			
							0	1	0	FIELD			
							0	1	1	DE			
							1	0	0	SFL			
		Reserved	0	0	0	0	0						

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes
			7	6	5	4	3	2	1	0		
0x6B	Output Sync Select 2	FLD_OUT_SEL[2:0] selects which sync comes out on the VS/FIELD/SFL pin						0	0	0	HSYNC	
								0	0	1	VSYNC	
								0	1	0	FIELD	
								0	1	1	DE	
								1	0	0	SFL	
	Reserved		0	0	0	1	0			Set as default		
0x8F	Free-Run Line Length 1	Reserved					0	0	0	0	Set as default	
		LLC_PAD_SEL[2:0]; enables manual selection of the clock for the LLC pin		0	0	0					LLC (nominal 27 MHz) selected out on LLC pin	
				1	0	1					LLC (nominal 13.5 MHz) selected out on LLC pin	
	Reserved		0							Sets to default		
0x99	CCAP1 (read only)	CCAP1[7:0]; closed caption data register	x	x	x	x	x	x	x	x	CCAP1[7] contains parity bit for Byte 0	
0x9A	CCAP2 (read only)	CCAP2[7:0]; closed caption data register	x	x	x	x	x	x	x	x	CCAP2[7] contains parity bit for Byte 0	
0x9B	Letterbox 1 (read only)	LB_LCT[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the top of active video	This feature examines the active video at the start and end of each field; it enables format detection even if the video is not accompanied by a CGMS or WSS sequence
0x9C	Letterbox 2 (read only)	LB_LCM[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected in the middle half of active video if subtitles are detected	
0x9D	Letterbox 3 (read only)	LB_LCB[7:0]; letterbox data register	x	x	x	x	x	x	x	x	Reports the number of black lines detected at the bottom of active video	
0xB2	CRC enable (write only)	Reserved							0	0	Sets as default	
		CRC_ENABLE; enable CRC checksum decoded from FMS packet to validate CGMSD						0			Turns off CRC check	
								1			CGMSD goes high with valid checksum	
	Reserved		0	0	0	1	1			Sets as default		
0xC3	ADC Switch 1	MUX0[2:0]; manual muxing control for MUX0; this setting controls which input is routed to the ADC for processing						0	0	0	No connect	MAN_MUX_EN = 1
								0	0	1	A <sub>IN</sub> 1	
								0	1	0	A <sub>IN</sub> 2	
								0	1	1	A <sub>IN</sub> 3	
								1	0	0	A <sub>IN</sub> 4	
			Reserved					0				
			MUX1[2:0]; manual muxing control for MUX1; this setting controls which input is routed to the ADC for processing		0	0	0				No connect	
					0	0	1				No connect	
					0	1	0				A <sub>IN</sub> 2	
			0	1	1				No connect			
			1	0	0				A <sub>IN</sub> 4			
	Reserved		0									
0xC4	ADC Switch 2	MUX2[2:0]; manual muxing control for MUX2; this setting controls which input is routed to the ADC for processing						0	0	0	No connect	MAN_MUX_EN = 1
								0	0	1	No connect	
								0	1	0	A <sub>IN</sub> 2	
								0	1	1	A <sub>IN</sub> 3	
								1	0	0	No connect	
			Reserved		0	0	0	0				
	MAN_MUX_EN; enable manual setting of input signal muxing		0						Disables	This bit must be set to 1 for manual muxing		
			1						Enables			
0xDC	Letterbox Control 1	LB_TH[4:0]; sets the threshold value that determines if a line is black				0	1	1	0	0	Default threshold for the detection of black lines 01101 to 10000—increase threshold, 00000 to 01011—decrease threshold	
		Reserved		1	0	1					Sets as default	

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes
			7	6	5	4	3	2	1	0		
0xDD	Letterbox Control 2	LB_EL[3:0]; programs the end line of the activity window for LB detection (end of field)					1	1	0	0	LB detection ends with the last line of active video on a field, 1100b: 262/525	
		LB_SL[3:0]; programs the start line of the activity window for LB detection (start of field)	1	1	0	0					Letterbox detection aligned with the start of active video, 0100b: 23/286 NTSC	
0xDE	ST Noise Readback 1 (read only)	ST_NOISE[10:8]						x	x	x		ST noise[10:0] measures the noise on the horizontal sync tip of video source
		ST_NOISE_VLD					x				When = 1, ST_NOISE[10:0] is valid	
0xDF	ST Noise Readback 2 (read only)	ST_NOISE[7:0]	x	x	x	x	x	x	x	x		
0xE1	SD offset Cb channel	SD_OFF_Cb[7:0]; adjusts the hue by selecting the offset for the Cb channel	0	0	0	0	0	0	0	0	-312 mV offset applied to the Cb channel	
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cb channel	
			1	1	1	1	1	1	1	1	1	+312 mV offset applied to the Cb channel
0xE2	SD offset Cr channel	SD_OFF_Cr[7:0]; adjusts the hue by selecting the offset for the Cr channel	0	0	0	0	0	0	0	0	-312 mV offset applied to the Cr channel	
			1	0	0	0	0	0	0	0	0 mV offset applied to the Cr channel	
			1	1	1	1	1	1	1	1	1	+312 mV offset applied to the Cr channel
0xE3	SD saturation Cb channel	SD_SAT_Cb[7:0]; adjusts the saturation by affecting gain on the Cb channel	0	0	0	0	0	0	0	0	Gain on Cb channel = -42 dB	
			1	0	0	0	0	0	0	0	Gain on Cb channel = 0 dB	
			1	1	1	1	1	1	1	1	1	Gain on Cb channel = +6 dB
0xE4	SD saturation Cr channel	SD_SAT_Cr[7:0]; adjusts the saturation by affecting gain on the Cr channel	0	0	0	0	0	0	0	0	Gain on Cr channel = -42 dB	
			1	0	0	0	0	0	0	0	Gain on Cr channel = 0 dB	
			1	1	1	1	1	1	1	1	1	Gain on Cr channel = +6 dB
0xE5	NTSC VSYNC begin	NVBEG[4:0]; number of lines after I <sub>COUNT</sub> rollover to set V high				0	0	1	0	1	NTSC default (ITU-R BT.656)	
		NVBEGSIGN			0						Sets to low when manual programming	
				1							Not suitable for user programming	
		NVBEGDELE; delay V bit going high by one line relative to NVBEG (even field)		0							No delay	
			1								Additional delay by one line	
0xE6	NTSC VSYNC end	NVEND[4:0]; number of lines after I <sub>COUNT</sub> rollover to set V low				0	0	1	0	0	NTSC default (ITU-R BT.656)	
		NVENDSIGN			0						Sets to low when manual programming	
				1							Not suitable for user programming	
		NVENDDELE; delay V bit going low by one line relative to NVEND (even field)		0							No delay	
			1								Additional delay by one line	
0xE7	NTSC FIELD toggle	NFTOG[4:0]; number of lines after I <sub>COUNT</sub> rollover to toggle F signal				0	0	0	1	1	NTSC default	
		NFTOGSIGN			0						Sets to low when manual programming	
				1							Not suitable for user programming	
		NFTOGDELE; delay F transition by one line relative to NFTOG (even field)		0							No delay	
			1								Additional delay by one line	
		NFTOGDELO; delay F transition by one line relative to NFTOG (odd field)	0								No delay	
			1								Additional delay by one line	

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes	
			7	6	5	4	3	2	1	0			
0xE8	PAL VSYNC begin	PVBEG[4:0]; number of lines after I <sub>COUNT</sub> rollover to set V high				0	0	1	0	1	PAL default (ITU-R BT.656)		
		PVBEGSIGN			0						Sets to low when manual programming		
					1							Not suitable for user programming	
		PVBEGDELE; delay V bit going high by one line relative to PVBEG (even field)		0								No delay	
				1								Additional delay by one line	
PVBEGDELO; delay V bit going high by one line relative to PVBEG (odd field)		0								No delay			
		1								Additional delay by one line			
0xE9	PAL VSYNC end	PVEND[4:0]; number of lines after I <sub>COUNT</sub> rollover to set V low.				1	0	1	0	0	PAL default (ITU-R BT.656)		
		PVENDSIGN			0						Sets to low when manual programming		
					1							Not suitable for user programming	
		PVENDDELE; delay V bit going low by one line relative to PVEND (even field)		0								No delay	
				1								Additional delay by one line	
PVENDDELO; delay V bit going low by one line relative to PVEND (odd field)		0								No delay			
		1								Additional delay by one line			
0xEA	PAL FIELD toggle	PFTOG[4:0]; number of lines after I <sub>COUNT</sub> rollover to toggle F signal				0	0	0	1	1	PAL default (ITU-R BT.656)		
		PFTOGSIGN			0						Sets to low when manual programming		
					1							Not suitable for user programming	
		PFTOGDELE; delay F transition by one line relative to PFTOG (even field)		0								No delay	
				1								Additional delay by one line	
PFTOGDELO; delay F transition by one line relative to PFTOG (odd field)		0								No delay			
		1								Additional delay by one line			
0xEB	Vblank Control 1	PVBIELCM[1:0]; PAL VBI even field line control							0	0	VBI ends one line earlier (Line 335)	Controls position of first active (comb filtered) line after VBI on even field in PAL	
									0	1	ITU-R BT.470 compliant (Line 336)		
									1	0	VBI ends one line later (Line 337)		
									1	1	VBI ends two lines later (Line 338)		
		PVBIOLCM[1:0]; PAL VBI odd field line control					0	0				VBI ends one line earlier (Line 22)	Controls position of first active (comb filtered) line after VBI on odd field in PAL
							0	1				ITU-R BT.470 compliant (Line 23)	
							1	0				VBI ends one line later (Line 24)	
							1	1				VBI ends two lines later (Line 25)	
		NVBIELCM[1:0]; NTSC VBI even field line control			0	0						VBI ends one line earlier (Line 282)	Controls position of first active (comb filtered) line after VBI on even field in NTSC
					0	1						ITU-R BT.470 compliant (Line 283)	
					1	0						VBI ends one line later (Line 284)	
					1	1						VBI ends two lines later (Line 285)	
		NVBIOLCM[1:0]; NTSC VBI odd field line control		0	0							VBI ends one line earlier (Line 20)	Controls position of first active (comb filtered) line after VBI on odd field in NTSC
	0		1							ITU-R BT.470 compliant (Line 21)			
	1		0							VBI ends one line later (Line 22)			
	1		1							VBI ends two lines later (Line 23)			



Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes			
			7	6	5	4	3	2	1	0					
0xEC	Vblank Control 2	PVBI ECCM[1:0]; PAL VBI even field color control								0	0	Color output beginning Line 335	Controls the position of first line that outputs color after VBI on even field in PAL		
										0	1	ITU-R BT.470 compliant color output beginning Line 336			
										1	0	Color output beginning Line 337			
										1	1	Color output beginning Line 338			
		PVBI OCCM[1:0]; PAL VBI odd field color control						0	0			Color output beginning Line 22		Controls the position of first line that outputs color after VBI on odd field in PAL	
								0	1			ITU-R BT.470-compliant color output beginning Line 23			
								1	0			Color output beginning Line 24			
								1	1			Color output beginning Line 25			
	NVBI ECCM[1:0]; NTSC VBI even field color control				0	0					Color output beginning Line 282	Controls the position of first line that outputs color after VBI on even field in NTSC			
					0	1					ITU-R BT.470-compliant color output beginning Line 283				
					1	0					VBI ends one line later (Line 284)				
					1	1					Color output beginning Line 285				
	NVBI OCCM[1:0]; NTSC VBI odd field color control		0	0							Color output beginning Line 20	Controls the position of first line that outputs color after VBI on odd field in NTSC			
			0	1							ITU-R BT.470 compliant color output beginning Line 21				
			1	0							Color output beginning Line 22				
			1	1							Color output beginning Line 23				
0xF3	AFE_CONTROL 1	AA_FILT_EN[3:0] antialiasing filter enable								0	Antialiasing Filter 1 disabled	AA_FILT_MAN_OVR must be enabled to change settings defined by INSEL[4:0]			
										1	Antialiasing Filter 1 enabled				
										0	Antialiasing Filter 2 disabled				
										1	Antialiasing Filter 2 enabled				
									0		Antialiasing Filter 3 disabled				
									1		Antialiasing Filter 3 enabled				
								0			Antialiasing Filter 4 enabled				
								1			Antialiasing Filter 4 enabled				
		AA_FILT_MAN_OVR; antialiasing filter override				0					Override disabled				
						1					Override enabled				
		0xF4	Drive strength	DR_STR_S[1:0]; selects the drive strength for the sync output signals							0		0	Low drive strength (1x)	
													0	1	
										1	0	Medium high drive strength (3x)			
										1	1	High drive strength (4x)			
DR_STR_C[1:0]; selects the drive strength for the clock output signal							0	0			Low drive strength (1x)				
								0	1			Medium low drive strength (2x)			
								1	0			Medium high drive strength (3x)			
								1	1			High drive strength (4x)			
DR_STR[1:0]; selects the drive strength for the data output signals; can be increased or decreased for EMC or crosstalk reasons						0	0					Low drive strength (1x)			
							0	1					Medium low drive strength (2x)		
							1	0					Medium high drive strength (3x)		
							1	1					High drive strength (4x)		
Reserved				x											
GLITCH_FILT_BYP	0														
	1														

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes	
			7	6	5	4	3	2	1	0			
0xF8	IF comp control	IFFILTSEL[2:0]; IF filter selection for PAL and NTSC						0	0	0	Bypass mode	0 dB	
			<b>2 MHz NTSC Filters</b>										
								0	0	1	-3 dB		
								0	1	0	-6 dB		
								0	1	1	-10 dB		
								1	0	0	Reserved		
			<b>3 MHz PAL Filters</b>										
								1	0	1	-2 dB		
								1	1	0	-5 dB		
								1	1	1	-7 dB		
	Reserved		0	0	0	0	0						
0xF9	VS mode control	EXTEND_VS_MAX_FREQ								0	Limits maximum VSYNC frequency to 66.25 Hz (475 lines/frame)		
										1	Limits maximum VSYNC frequency to 70.09 Hz (449 lines/frame)		
		EXTEND_VS_MIN_FREQ								0	Limits minimum VSYNC frequency to 42.75 Hz (731 lines/frame)		
										1	Limits minimum VSYNC frequency to 39.51 Hz (791 lines/frame)		
		VS_COAST_MODE[1:0]					0	0			Autocoast mode		This value sets up the output coast frequency
							0	1			50 Hz coast mode		
							1	0			60 Hz coast mode		
							1	1			Reserved		
	Reserved		0	0	0	0							
0xFB	Peaking gain	PEAKING_GAIN[7:0]	0	1	0	0	0	0	0	0	Increases/decreases the gain for high frequency portions of the video signal		
0xFC	DNR Noise Threshold 2	DNR_TH2[7:0]	0	0	0	0	0	1	0	0	Specifies the maximum luma edge that is interpreted as noise and therefore blanked		
0xFE	CSI Tx slave address	Reserved								0	Reserved		
		CSI_TX_SLAVE_ADDR[6:0]	0	0	0	0	0	0	0	0	0	Programs the I <sup>2</sup> C address of the MIPI CSI TX	

<sup>1</sup>x indicates a bit that keeps the last written value.

To access the registers listed in Table 95, SUB\_USR\_EN in Register Address 0x0E must be programmed to 10b. The gray shading is the default.

Table 95. Register Map Descriptions User Sub Map 2

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)							Comments	Notes		
			7	6	5	4	3	2	1			0	
0x80	ACE Control 1	Reserved		0	0	0	0	0	0	0	0	Reserved.	
		ACE_ENABLE	0									Disable ACE.	
0x83	ACE Control 4	ACE_LUMA_GAIN[4:0]				0	1	1	0	1		Set ACE luma auto-contrast level to default value. 5b'00000 minimum value ... 5b'11111 maximum value	When ACE_ENABLE is set to 1
		Reserved	0	0	0								
0x84	ACE Control 5	ACE_CHROMA_GAIN[3:0]					1	0	0	0		Set ACE color auto-saturation level 4b'0000 minimum value ... 4b'1111 maximum value	
		ACE_CHROMA_MAX[3:0]	1	0	0	0						Set maximum threshold for ACE color color-saturation level 4b'0000 = minimum value ... 4b'1111 = maximum value	
0x85	ACE Control 6	ACE_GAMMA_GAIN[3:0]					1	0	0	0		Set further contrast enhancement 4b'0000 = minimum value ... 4b'1111 = maximum value	
		ACE_RESPONSE_SPEED[3:0]	1	1	1	1						Sets speed of ACE response 4b'0000 slowest value ... 4b'1111 fastest value	
0x92	Dither control	BR_DITHER_MODE									0	8-bit to 6-bit down dither disabled	
		Reserved	0	0	0	0	0	0	0	0	1	8-bit to 6-bit down dither enabled	
0xD9	Min Max 0	MIN_THRESH_Y[7:0]	0	0	0	0	0	0	0	0	0	Selects the minimum threshold for the incoming luma video signal.	
0xDA	Min Max 1	MAX_THRESH_Y[7:0]	1	1	1	1	1	1	1	1	1	Selects the maximum threshold for the incoming luma video signal.	
0xDB	Min Max 2	MIN_THRESH_C[7:0]	0	0	0	0	0	0	0	0	0	Selects the minimum threshold for the incoming chroma video signal.	
0xDC	Min Max 3	MAX_THRESH_C[7:0]	1	1	1	1	1	1	1	1	1	Selects the maximum threshold for the incoming chroma video signal.	
0xDD	Min Max 4	MAX_SAMPLES_ALLOWED_Y[3:0]					1	1	0	0		Selects the number of maximum luma samples allowed in a given window before an interrupt is triggered.	
		MIN_SAMPLES_ALLOWED_Y[3:0]	1	1	0	0						Selects the number of minimum luma samples allowed in a given window before an interrupt is triggered.	
0xDE	Min Max 5	MAX_SAMPLES_ALLOWED_C[3:0]					1	1	0	0		Selects the number of maximum chroma samples allowed in a given window before an interrupt is triggered.	
		MIN_SAMPLES_ALLOWED_C[3:0]	1	1	0	0						Selects the number of minimum chroma samples allowed in a given window before an interrupt is triggered.	
0xE0	FL Control	FL_ENABLE									0		
		Reserved	0	0	0	0	0	0	0	0	1	Enables fast lock.	
0xE1	Y Average 0	LINE_START[8:1]	0	0	0	1	0	0	0	0	1	Selects starting line for field averaging.	See Subaddress 0xE5 for least significant bits
0xE2	Y Average 1	LINE_END[8:1]	1	0	0	0	1	0	0	0	Selects end line for field averaging.		
0xE3	Y Average 2	SAMPLE_START[9:2]	0	0	0	1	0	1	1	1	Selects starting sample for line averaging.		
0xE4	Y Average 3	SAMPLE_END[9:2]	1	1	0	1	0	1	1	1	Selects end sample for line averaging.		

Subaddress	Register	Bit Description	Bits (Shading Indicates Default State)								Comments	Notes	
			7	6	5	4	3	2	1	0			
0xE5	Y Average 4	LINE_START[0]									1		
		LINE_END[0]									1		
		Reserved						0	0				
		SAMPLE_START[1:0]			1	0							
		SAMPLE_END[1:0]	0	0									
0xE6	Y Average 5	CAPTURE_VALUE									0	Trigger used to store the readback value.	
		Y_AVG_FILT_EN									0	Enable low pass filtering of the y_averaged signal.	
		Y_AVG_TIME_CONST[2:0]				1	0	0				Selects the filter cutoff to be used for filtering the y averaged data. 3'b1xx = least filtered. 3'b000 = next least. ... 3'b011 = heavily filtered.	
		Reserved	0	0	0								
0xE7	Y Average Data MSB	Y_AVERAGE[9:2]	x	x	x	x	x	x	x	x	x	Contains the averaged video data.	Note these are read only registers
0xE8	Y Average Data LSB	Y_AVERAGE[1:0]								x	x		

To access the registers listed in Table 96, SUB\_USR\_EN in Register Address 0x0E must be programmed to 01b. The gray shading is the default.

**Table 96. Interrupt/VDP Map Descriptions<sup>1</sup>**

Interrupt/VDP Map			Bit (Shading Indicates Default State)								Comments	Notes		
Address	Register	Bit Description	7	6	5	4	3	2	1	0				
0x40	Interrupt Configuration 1	INTRQ_OP_SEL[1:0]; interrupt drive level select							0	0	Open drain			
										0	1		Drive low when active	
											1		0	Drive high when active
											1		1	Reserved
		MPU_STIM_INTRQ; manual interrupt set mode									0			Manual interrupt mode disabled
											1			Manual interrupt mode enabled
		Reserved						x						Not used
		MV_INTRQ_SEL[1:0]; Macrovision interrupt select				0	0							Reserved
							0	1						Pseudo sync only
								1	0					Color stripe only
								1	1					Pseudo sync or color stripe
		INTRQ_DUR_SEL[1:0]; interrupt duration select		0	0									Three XTAL periods
				0	1									15 XTAL periods
	1		0								63 XTAL periods			
	1		1								Active until cleared			
0x42	Interrupt Status 1 (read only)	SD_LOCK_Q								0	No change	These bits can be cleared or masked in Register 0x43 and Register 0x44, respectively		
											1		SD input has caused the decoder to go from an unlocked state to a locked state	
		SD_UNLOCK_Q									0		No change	
													1	SD input has caused the decoder to go from a locked state to an unlocked state
		Reserved					x	x	x					
		SD_FR_CHNG_Q				0								No change
							1							Denotes a change in the free-run status
		MV_PS_CS_Q		0										No change
			1								Pseudo sync/color striping detected; see Register 0x40 MV_INTRQ_SEL[1:0] for selection			
Reserved		x												
0x43	Interrupt Clear 1 (write only)	SD_LOCK_CLR								0	Do not clear			
											1		Clears SD_LOCK_Q bit	
		SD_UNLOCK_CLR									0		Do not clear	
													1	Clears SD_UNLOCK_Q bit
		Reserved					0	0	0				Not used	
		SD_FR_CHNG_CLR			0									Do not clear
						1								Clears SD_FR_CHNG_Q bit
		MV_PS_CS_CLR		0										Do not clear
			1								Clears MV_PS_CS_Q bit			
Reserved		x									Not used			
0x44	Interrupt Mask 1 (read/write)	SD_LOCK_MSK								0	Masks SD_LOCK_Q bit			
											1		Unmasks SD_LOCK_Q bit	
		SD_UNLOCK_MSK									0		Masks SD_UNLOCK_Q bit	
													1	Unmasks SD_UNLOCK_Q bit
		Reserved					0	0	0				Not used	
		SD_FR_CHNG_MSK			0									Masks SD_FR_CHNG_Q bit
						1								Unmasks SD_FR_CHNG_Q bit
		MV_PS_CS_MSK		0										Masks MV_PS_CS_Q bit
			1								Unmasks MV_PS_CS_Q bit			
Reserved		x									Not used			

Interrupt/VDP Map			Bit (Shading Indicates Default State)								Comments	Notes	
Address	Register	Bit Description	7	6	5	4	3	2	1	0			
0x45	Raw Status 2 (read only)	CCAPD								0	No CCAPD data detected—VBI System 2	These bits are status bits only; they cannot be cleared or masked; Register 0x46 is used for this purpose	
										1	CCAPD data detected—VBI System 2		
		Reserved					x	x	x				
		EVEN_FIELD				0							Current SD field is odd numbered
					1								Current SD field is even numbered
		CHX_MIN_MAX_INTRQ			0								If the input to the ADC is within the correct range this is 0
					1								If the input to the ADC is outside the range this is set to 1. The range is set by User Sub Map 2
		Reserved			x								Not used
		MPU_STIM_INTRQ			0								MPU_STIM_INTRQ = 0
			1							MPU_STIM_INTRQ = 1			
0x46	Interrupt Status 2 (read only)	CCAPD_Q								0	Closed captioning not detected in the input video signal—VBI System 2	These bits can be cleared or masked by Register 0x47 and Register 0x48, respectively; note that the interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer	
										1	Closed captioning data detected in the video input signal—VBI System 2		
		Reserved								x			Not used
		Reserved					x	x					Not used
		SD_FIELD_CHNGD_Q				0							SD signal has not changed field from odd to even or vice versa
					1								SD signal has changed Field from odd to even or vice versa
		Reserved			x	x							Not used
		MPU_STIM_INTRQ_Q			0								Manual interrupt not set
			1							Manual interrupt set			
0x47	Interrupt Clear 2 (write only)	CCAPD_CLR								0	Do not clear—VBI System 2	Note that interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer	
										1	Clears CCAPD_Q bit—VBI System 2		
		Reserved								x			Not used
		Reserved					x	x					
		SD_FIELD_CHNGD_CLR				0							Do not clear
					1								Clears SD_FIELD_CHNGD_Q bit
		CHX_MIN_MAX_INTRQ_CLR				0							Do not clear
					1								Clears CHX_MIN_MAX_INTRQ bit
		Reserved			x								Not used
MPU_STIM_INTRQ_CLR			0							Do not clear			
			1							Clears MPU_STIM_INTRQ_Q bit			

Interrupt/VDP Map			Bit (Shading Indicates Default State)								Comments	Notes	
Address	Register	Bit Description	7	6	5	4	3	2	1	0			
0x48	Interrupt Mask 2 (read/write)	CCAPD_MSK								0	Masks CCAPD_Q bit—VBI System 2	Note that interrupt in Register 0x46 for the CCAP, CGMS, and WSS data uses the Mode 1 data slicer	
										1	Unmasks CCAPD_Q bit—VBI System 2		
		Reserved									0		Not used
		Reserved						0	0				Not used
		SD_FIELD_CHNGD_MSK				0							Masks SD_FIELD_CHNGD_Q bit
							1						Unmasks SD_FIELD_CHNGD_Q bit
		CHX_MIN_MAX_INTRQ_MSKB			0								Masks CHX_MIN_MAX_INTRQ bit
						1							Unmasks CHX_MIN_MAX_INTRQ bit
		Reserved			0								Not used
MPU_STIM_INTRQ_MSK			0								Masks MPU_STIM_INTRQ_Q bit		
			1								Unmasks MPU_STIM_INTRQ_Q bit		
0x49	Raw Status 3 (read only)	SD_OP_50Hz; SD 60 Hz/50 Hz frame rate at output								0	SD 60 Hz signal output	These bits are status bits only; they cannot be cleared or masked; Register 0x4A is used for this purpose	
										1	SD 50 Hz signal output		
		SD_V_LOCK									0		SD vertical sync lock is not established
											1		SD vertical sync lock established
		SD_H_LOCK									0		SD horizontal sync lock is not established
											1		SD horizontal sync lock established
		Reserved						x					Not used
		SCM_LOCK					0						SECAM lock is not established
							1						SECAM lock established
Reserved	x	x	x							Not used			
0x4A	Interrupt Status 3 (read only)	SD_OP_CHNG_Q; SD 60 Hz/50 Hz frame rate at output									0	No change in SD signal standard detected at the output	These bits can be cleared and masked by Register 0x4B and Register 0x4C, respectively
											1	A change in SD signal standard is detected at the output	
		SD_V_LOCK_CHNG_Q									0	No change in SD VSYNC lock status	
											1	SD VSYNC lock status has changed	
		SD_H_LOCK_CHNG_Q									0	No change in HSYNC lock status	
											1	SD HSYNC lock status has changed	
		SD_AD_CHNG_Q; SD autodetect changed						0				No change in AD_RESULT[2:0] bits in Status 1 register	
								1				AD_RESULT[2:0] bits in Status 1 register have changed	
		SCM_LOCK_CHNG_Q; SECAM lock					0					No change in SECAM lock status	
								1				SECAM lock status has changed	
		PAL_SW_LK_CHNG_Q				0						No change in PAL swinging burst lock status	
								1				PAL swinging burst lock status has changed	
		Reserved	x	x								Not used	

Interrupt/VDP Map			Bit (Shading Indicates Default State)								Comments	Notes					
Address	Register	Bit Description	7	6	5	4	3	2	1	0							
0x4B	Interrupt Clear 3 (write only)	SD_OP_CHNG_CLR								0	Do not clear						
										1	Clears SD_OP_CHNG_Q bit						
		SD_V_LOCK_CHNG_CLR									0		Do not clear				
											1		Clears SD_V_LOCK_CHNG_Q bit				
		SD_H_LOCK_CHNG_CLR									0		Do not clear				
											1		Clears SD_H_LOCK_CHNG_Q bit				
		SD_AD_CHNG_CLR									0		Do not clear				
											1		Clears SD_AD_CHNG_Q bit				
0x4C	Interrupt Mask 3 (read/write)	SD_OP_CHNG_MSK									0	Masks SD_OP_CHNG_Q bit					
											1	Unmasks SD_OP_CHNG_Q bit					
		SD_V_LOCK_CHNG_MSK										0		Masks SD_V_LOCK_CHNG_Q bit			
												1		Unmasks SD_V_LOCK_CHNG_Q bit			
		SD_H_LOCK_CHNG_MSK										0		Masks SD_H_LOCK_CHNG_Q bit			
												1		Unmasks SD_H_LOCK_CHNG_Q bit			
		SD_AD_CHNG_MSK										0		Masks SD_AD_CHNG_Q bit			
												1		Unmasks SD_AD_CHNG_Q bit			
0x4E	Interrupt Status 4 (read only)	VDP_CCAPD_Q										0	Closed captioning not detected	These bits can be cleared and masked by Register 0x4F and Register 0x50, respectively; note that an interrupt in Register 0x4E for the CCAP, CGMS, and WSS data uses the VDP data slicer			
												1	Closed captioning detected				
		Reserved											x				
		VDP_CGMS_WSS_CHNGD_Q; see Address 0x9C, Bit 4, of User Sub Map to determine whether interrupt is issued for a change in detected data or for when data is detected, regardless of content											0		CGMS/WSS data is not changed/not available		
													1		CGMS/WSS data is changed/available		
		Reserved													x		
		Reserved														x	
		Reserved														x	
Reserved													x				
Reserved													x				



Interrupt/VDP Map			Bit (Shading Indicates Default State)								Comments	Notes		
Address	Register	Bit Description	7	6	5	4	3	2	1	0				
0x4F	Interrupt Clear 4 (write only)	VDP_CCAPD_CLR								0	Do not clear	In Register 0x4E, CCAP/CGMS/WSS data uses VDP data slicer		
										1	Clears VDP_CCAPD_Q			
		Reserved									0			
		VDP_CGMS_WSS_CHNGD_CLR									0		Do not clear	
											1		Clears VDP_CGMS_WSS_CHNGD_Q	
		Reserved									0			
		Reserved									0			
		Reserved									0			
		Reserved									0		Do not clear	
		Reserved									0			
0x50	Interrupt Mask 4	VDP_CCAPD_MSK									0	Masks VDP_CCAPD_Q	Note that an interrupt in Register 0x4E for the CCAP, CGMS, and WSS data uses the VDP data slicer	
											1	Unmasks VDP_CCAPD_Q		
		Reserved									0			
		VDP_CGMS_WSS_CHNGD_MSK										0		Masks VDP_CGMS_WSS_CHNGD_Q
												1		Unmasks VDP_CGMS_WSS_CHNGD_Q
		Reserved									0			
		Reserved									0			
		Reserved									0			
		Reserved									0			
		Reserved									0			
0x51	Interrupt Latch 0 (read only)	CR_CHANNEL_MAX_VIOLATION									0	Cr value is below programmed maximum value	This register is cleared by CHX_MIN_MAX_INTRQ_CLR	
											1	Cr value is above programmed maximum value		
		CR_CHANNEL_MIN_VIOLATION										0		Cr value is above programmed minimum value
												1		Cr value is below programmed minimum value
		CB_CHANNEL_MAX_VIOLATION										0		Cb value is below programmed maximum value
												1		Cb value is above programmed maximum value
		CB_CHANNEL_MIN_VIOLATION										0		Cb value is above programmed minimum value
												1		Cb value is below programmed minimum value
		Y_CHANNEL_MAX_VIOLATION										0		Y value is below programmed maximum value
												1		Y value is above programmed maximum value
		Y_CHANNEL_MIN_VIOLATION										0		Y value is above programmed minimum value
												1		Y value is below programmed minimum value
		Reserved										0		
		Reserved										0		

Interrupt/VDP Map			Bit (Shading Indicates Default State)								Comments	Notes	
Address	Register	Bit Description	7	6	5	4	3	2	1	0			
0x60	VDP_CONFIG_1	VDP_TTXT_TYPE_MAN[1:0]							0	0	PAL: Teletext-ITU-BT.653-625/50-A, NTSC: reserved		
									0	1	PAL: Teletext-ITU-BT.653-625/50-B (WST), NTSC: Teletext-ITU-BT.653-525/60-B		
									1	0	PAL: Teletext-ITU-BT.653-625/50-C, NTSC: Teletext-ITU-BT.653-525/60-C, or EIA516 (NABTS)		
									1	1	PAL: Teletext-ITU-BT.653-625/50-D, NTSC: Teletext-ITU-BT.653-525/60-D		
		VDP_TTXT_TYPE_MAN_ENABLE								0			User programming of teletext type disabled
										1			User programming of teletext type enabled
		WST_PKT_DECODE_DISABLE								0			Enables hamming decoding of WST packets
										1			Disables hamming decoding of WST packets
Reserved			1	0	0	0							
0x62	VDP_ADF_CONFIG_1	ADF_DID[4:0]				1	0	1	0	1	User-specified DID sent in the ancillary data stream with VDP decoded data	Sets whether ancillary data output mode in byte mode or nibble mode	
			ADF_MODE[1:0]		0	0							Nibble mode
				0	1						Byte mode, no code restrictions		
				1	0						Byte mode with 0x00 and 0xFF prevented		
				1	1						Reserved		
		ADF_ENABLE	0										Disables insertion of VBI decoded data into ancillary 656 stream
1										Enables insertion of VBI decoded data into ancillary 656 stream			
0x63	VDP_ADF_CONFIG_2	ADF_SDID[5:0]			1	0	1	0	1	0	User-specified SDID sent in the ancillary data stream with VDP decoded data		
			Reserved			x							
		DUPLICATE_ADF	0										Ancillary data packet is spread across the Y and C data streams
			1										Ancillary data packet is duplicated on the Y and C data streams
0x64	VDP_LINE_00E	VBI_DATA_P318[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 318 (PAL), NTSC—not applicable		
			Reserved			0	0	0					
		MAN_LINE_PGM	0										Decode default standards on the lines indicated in Table 74
1										Manually program the VBI standard to be decoded on each line; see Table 75	If set to 1, all VBI_DATA_Px_Ny bits can be set as desired		
0x65	VDP_LINE_00F	VBI_DATA_P319_N286[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 319 (PAL), Line 286 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective	
			VBI_DATA_P6_N23[3:0]	0	0	0	0				Sets VBI standard to be decoded from Line 6 (PAL), Line 23 (NTSC)		

Interrupt/VDP Map			Bit (Shading Indicates Default State)								Comments	Notes
Address	Register	Bit Description	7	6	5	4	3	2	1	0		
0x66	VDP_LINE_010	VBI_DATA_P320_N287[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 320 (PAL), Line 287 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P7_N24[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 7 (PAL), Line 24 (NTSC)	
0x67	VDP_LINE_011	VBI_DATA_P321_N288[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 321 (PAL), Line 288 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P8_N25[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 8 (PAL), Line 25 (NTSC)	
0x68	VDP_LINE_012	VBI_DATA_P322[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 322 (PAL), NTSC—not applicable	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P9[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 9 (PAL), NTSC—not applicable	
0x69	VDP_LINE_013	VBI_DATA_P323[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 323 (PAL), NTSC—not applicable	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 10 (PAL), NTSC—not applicable	
0x6A	VDP_LINE_014	VBI_DATA_P324_N272[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 324 (PAL), Line 272 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 11 (PAL); NTSC—not applicable	
0x6B	VDP_LINE_015	VBI_DATA_P325_N273[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 325 (PAL), Line 273 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P12_N10[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 12 (PAL), Line 10 (NTSC)	
0x6C	VDP_LINE_016	VBI_DATA_P326_N274[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 326 (PAL), Line 274 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P13_N11[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 13 (PAL), Line 11 (NTSC)	
0x6D	VDP_LINE_017	VBI_DATA_P327_N275[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 327 (PAL), Line 275 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P14_N12[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 14 (PAL), Line 12 (NTSC)	
0x6E	VDP_LINE_018	VBI_DATA_P328_N276[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 328 (PAL), Line 276 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P15_N13[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 15 (PAL), Line 13 (NTSC)	
0x6F	VDP_LINE_019	VBI_DATA_P329_N277[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 329 (PAL), Line 277 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P16_N14[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 16 (PAL), Line 14 (NTSC)	

Interrupt/VDP Map			Bit (Shading Indicates Default State)								Comments	Notes
Address	Register	Bit Description	7	6	5	4	3	2	1	0		
0x70	VDP_LINE_01A	VBI_DATA_P330_N278[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 330 (PAL), Line 278 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P17_N15[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 17 (PAL), Line 15 (NTSC)	
0x71	VDP_LINE_01B	VBI_DATA_P331_N279[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 331 (PAL), Line 279 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P18_N16[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 18 (PAL), Line 16 (NTSC)	
0x72	VDP_LINE_01C	VBI_DATA_P332_N280[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 332 (PAL), Line 280 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P19_N17[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 19 (PAL), Line 17 (NTSC)	
0x73	VDP_LINE_01D	VBI_DATA_P333_N281[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 333 (PAL), Line 281 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P20_N18[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 20 (PAL), Line 18 (NTSC)	
0x74	VDP_LINE_01E	VBI_DATA_P334_N282[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 334 (PAL), Line 282 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P21_N19[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 21 (PAL), Line 19 (NTSC)	
0x75	VDP_LINE_01F	VBI_DATA_P335_N283[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 335 (PAL), Line 283 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P22_N20[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 22 (PAL), Line 20 (NTSC)	
0x76	VDP_LINE_020	VBI_DATA_P336_N284[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 336 (PAL), Line 284 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P23_N21[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 23 (PAL), Line 21 (NTSC)	
0x77	VDP_LINE_021	VBI_DATA_P337_N285[3:0]					0	0	0	0	Sets VBI standard to be decoded from Line 337 (PAL), Line 285 (NTSC)	MAN_LINE_PGM must be set to 1 for these bits to be effective
		VBI_DATA_P24_N22[3:0]	0	0	0	0					Sets VBI standard to be decoded from Line 24 (PAL), Line 22 (NTSC)	

Interrupt/VDP Map			Bit (Shading Indicates Default State)								Comments	Notes	
Address	Register	Bit Description	7	6	5	4	3	2	1	0			
0x78	VDP_STATUS (read only)	CC_AVL								0	Closed captioning not detected	CC_CLEAR resets the CC_AVL bit	
										1	Closed captioning is detected		
		CC_EVEN_FIELD									0	Closed captioning decoded from odd field	
											1	Closed captioning decoded from even field	
		CGMS_WSS_AVL									0	CGMS/WSS is not detected	CGMS_WSS_CLEAR resets the CGMS_WSS_AVL bit
											1	CGMS/WSS detected	
	Reserved			0	0	0	0						
	TTXT_AVL			0								Teletext not detected	
				1								Teletext detected	
	VDP_STATUS_CLEAR (write only)	CC_CLEAR									0	Does not reinitialize the CCAP readback registers	This is a self-clearing bit
											1	Reinitializes the CCAP readback registers	
		Reserved									0		
CGMS_WSS_CLEAR											0	Does not reinitialize the CGMS/WSS readback registers	This is a self-clearing bit
											1	Reinitializes the CGMS/WSS readback registers	
Reserved			0	0	0	0	0						
0x79	VDP_CCAP_DATA_0 (read only)	CCAP_BYTE_1[7:0]	x	x	x	x	x	x	x	x	Decoded Byte 1 of CCAP		
0x7A	VDP_CCAP_DATA_1 (read only)	CCAP_BYTE_2[7:0]	x	x	x	x	x	x	x	x	Decoded Byte 2 of CCAP		
0x7D	VDP_CGMS_WSS_DATA_0 (read only)	CGMS_CRC[5:2]					x	x	x	x	Decoded CRC sequence for CGMS		
		Reserved	0	0	0	0							
0x7E	VDP_CGMS_WSS_DATA_1 (read only)	CGMS_WSS[13:8]			x	x	x	x	x	x	Decoded CGMS/WSS data		
		CGMS_CRC[1:0]	x	x								Decoded CRC sequence for CGMS	
0x7F	VDP_CGMS_WSS_DATA_2 (read only)	CGMS_WSS[7:0]	x	x	x	x	x	x	x	x	Decoded CGMS/WSS data		
0x9C	VDP_OUTPUT_SEL	Reserved						0	0	0	0		
		WSS_CGMS_CB_CHANGE				0						Disable content-based updating of CGMS and WSS data	The available bit shows the availability of data only when its content has changed
						1						Enable content-based updating of CGMS and WSS data	
Reserved			0	0	0								

<sup>1</sup> x indicates a bit that keeps the last written value.

## PCB LAYOUT RECOMMENDATIONS

The [ADV7182](#) is a high precision, high speed, mixed-signal device. To achieve the maximum performance from the part, it is important to have a well laid out PCB. The following is a guide for designing a board using the [ADV7182](#).

### ANALOG INTERFACE INPUTS

Take care when routing the inputs on the PCB. Keep track lengths to a minimum and use  $75\ \Omega$  trace impedances when possible because trace impedances other than  $75\ \Omega$  increase the chance of reflections.

### POWER SUPPLY DECOUPLING

It is recommended that each power supply pin be decoupled with  $0.1\ \mu\text{F}$  and  $10\ \text{nF}$  capacitors. The fundamental idea is to have a decoupling capacitor within about  $0.5\ \text{cm}$  of each power pin. In addition, avoid placing the capacitor on the opposite side of the PCB from the [ADV7182](#) because doing so interposes inductive vias in the path. Locate the decoupling capacitors between the power plane and the power pin. Flow current from the power plane to the capacitor and then to the power pin. Do not apply the power connection between the capacitor and the power pin. Placing a via underneath the  $100\ \text{nF}$  capacitor pads, down to the power plane, is the best approach (see Figure 48).

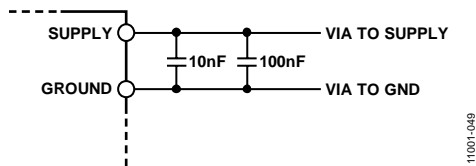


Figure 48. Recommended Power Supply Decoupling

It is particularly important to maintain low noise and good stability of PVDD. Pay careful attention to regulation, filtering, and decoupling. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (AVDD, DVDD, DVDDIO, and PVDD).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can in turn produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least  $P_{VDD}$ , from a different, cleaner power source, for example, from a  $12\ \text{V}$  supply.

Using a single ground plane for the entire board is also recommended.

Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

### VREFN AND VREFP

Place the circuit associated with the VREFN and VREFP pins as close as possible and on the same side of the PCB as the [ADV7182](#).

### DIGITAL OUTPUTS (BOTH DATA AND CLOCKS)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, requiring more current and, in turn, causing more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a  $30\ \Omega$  to  $50\ \Omega$  series resistor can suppress reflections, reduce EMI, and reduce the current spikes inside the [ADV7182](#). If series resistors are used, place them as close as possible to the [ADV7182](#) pins. However, try not to add vias or extra length to the output trace to place the resistors closer.

If possible, limit the capacitance that each of the digital outputs drives to less than  $15\ \text{pF}$ . This can be accomplished easily by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the [ADV7182](#), creating more digital noise on its power supplies.

The [ADV7182](#) has an exposed metal paddle on the bottom of the package. This paddle must be soldered to PCB ground for proper heat dissipation and for noise and mechanical strength benefits.

### DIGITAL INPUTS

The digital inputs on the [ADV7182](#) are designed to work with  $1.8\ \text{V}$  to  $3.3\ \text{V}$  signals and are not tolerant of  $5\ \text{V}$  signals. Extra components are needed if  $5\ \text{V}$  logic signals are required to be applied to the decoder.

# TYPICAL CIRCUIT CONNECTION

Figure 49 provides an example of how to connect the [ADV7182](#). For a detailed schematic of the [ADV7182](#) evaluation boards, contact a local Analog Devices field applications engineer or Analog Devices distributor.

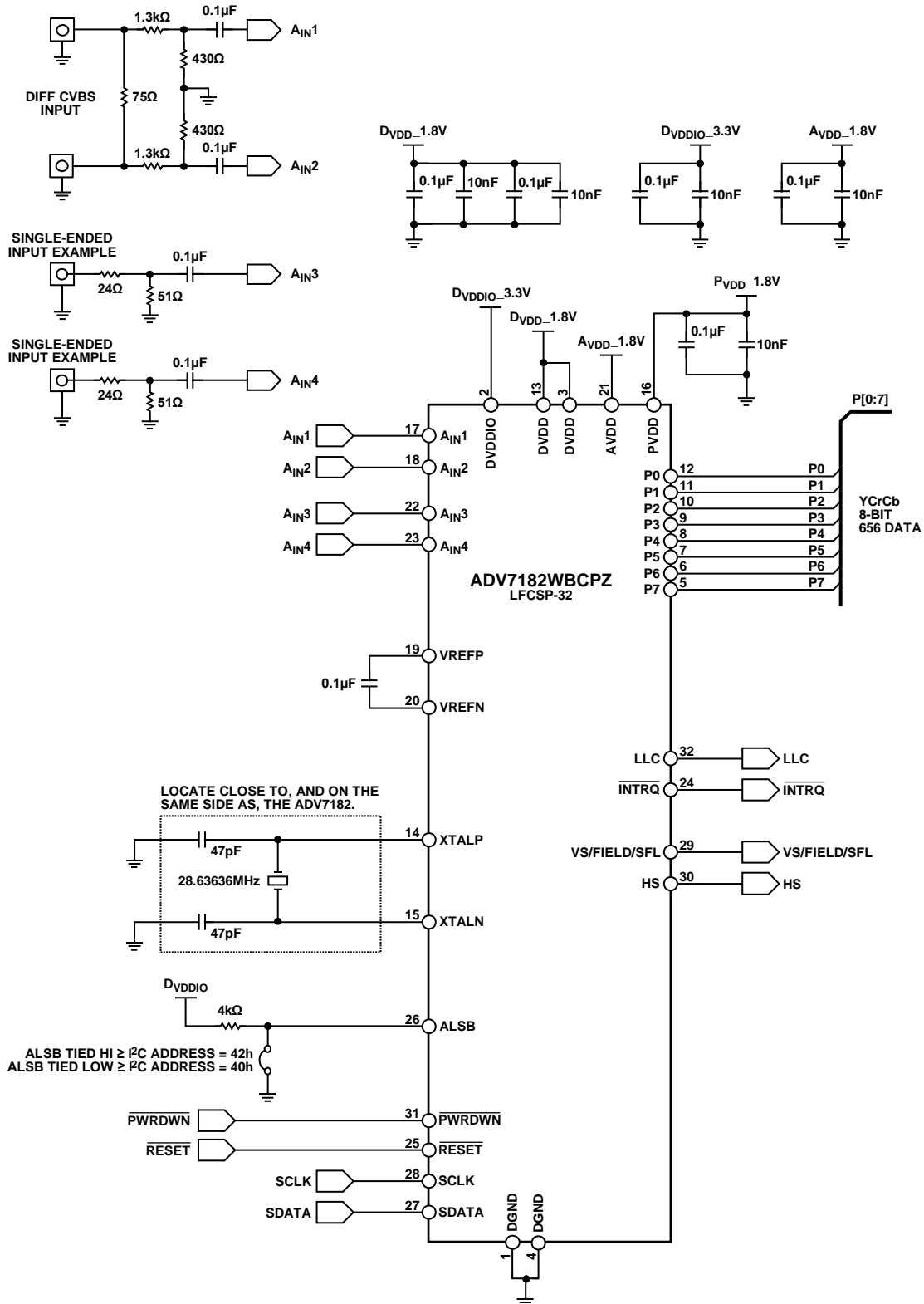
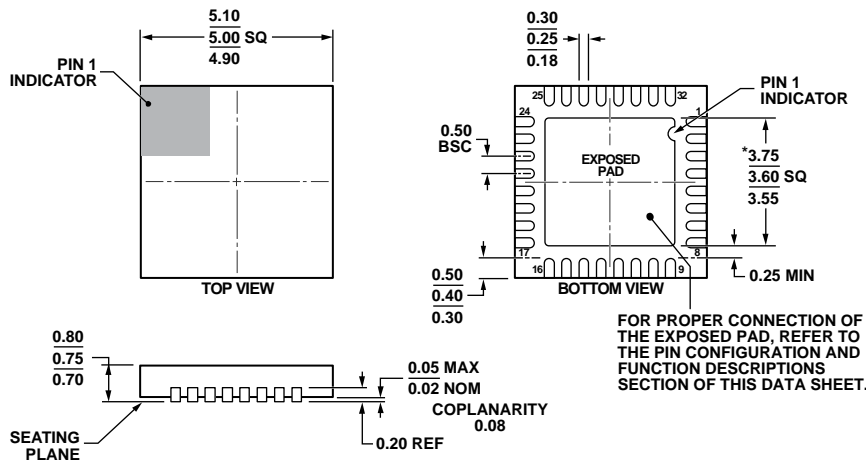


Figure 49. [ADV7182](#) Typical Connection Diagram

OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-5 WITH EXCEPTION TO EXPOSED PAD DIMENSION.

Figure 50. 32-Lead Lead Frame Chip Scale Package [LFCSP\_WQ]  
 5 mm × 5 mm Body, Very Very Thin Quad  
 (CP-32-12)  
 Dimensions shown in millimeters

09-16-2010-B

ORDERING GUIDE

Model <sup>1,2</sup>	Temperature Range	Package Description	Package Option
ADV7182WBCPZ	-40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
ADV7182WBCPZ-RL	-40°C to +105°C	32-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-32-12
EVAL-ADV7182EBZ		Evaluation Board for the 32-Lead LFCSP	

<sup>1</sup> Z = RoHS Compliant Part.  
<sup>2</sup> W = Qualified for Automotive Applications.

AUTOMOTIVE PRODUCTS

The ADV7182W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

I<sup>2</sup>C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).